

## FEATURES

### ■ Video Decoder

- Supports NTSC and PAL video input formats
- 2D NTSC and PAL comb-filter for Y/C separation of CVBS input
- Single CVBS and S-video input
- Supports Closed-caption and V-chip
- ACC, AGC, and DCGC (Digital Chroma Gain Control)

### ■ Color Engine

- Brightness, contrast, saturation, and hue adjustment
- 9-tap programmable multi-purpose FIR (Finite Impulse Response) filter
- Differential 3-band peaking engine
- Luminance Transient Improvement (LTI)
- Chrominance Transient Improvement (CTI)
- Black Level Extension (BLE)
- White Level Extension (WLE)
- Favor Color Compensation (FCC)
- 3-channel gamma curve adjustment

### ■ Scaling Engine/TCON

- Supports analog panels with the resolution of 960x234, 1200x234, 1400x234, and more
- Supports various displaying modes
- Supports horizontal panorama scaling

### ■ Digital PWM Controller

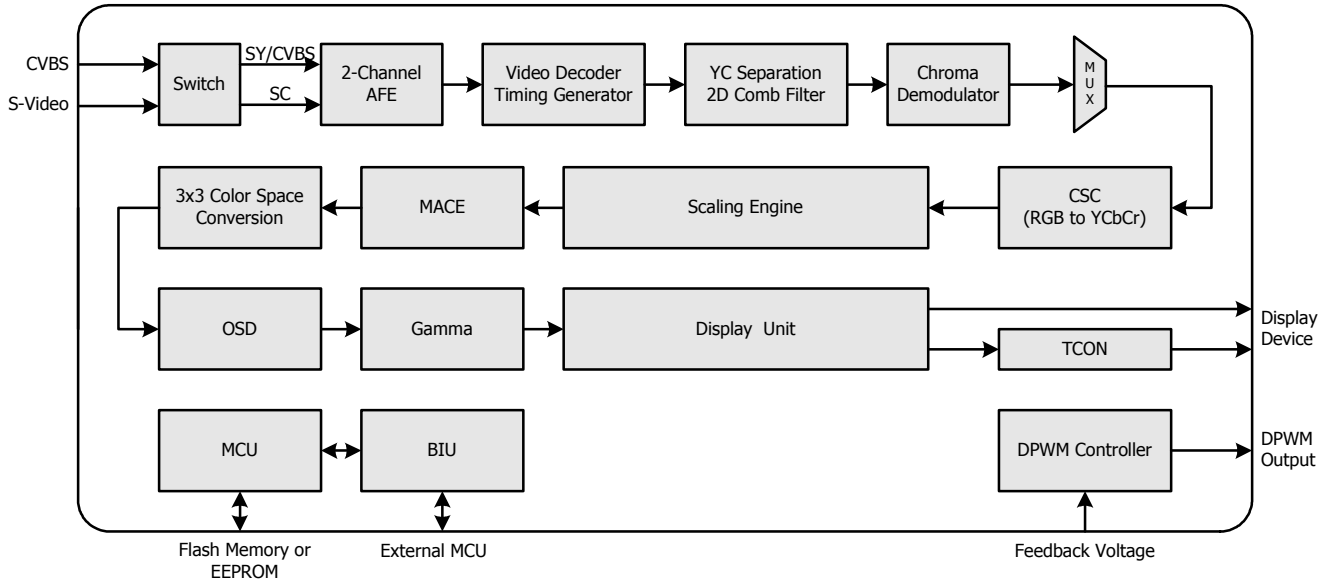
- Integrated general purpose digital PWM control loop

- Programmable startup operating frequency and period with output voltage regulation
- Programmable output current regulation; 40KHz~70KHz switching frequency, sync. to HSYNC possible
- Burst-mode or continuous-mode for output current regulation; 150Hz~300Hz burst-mode frequency, sync. to VSYNC possible
- Programmable protection level for input voltage and fault detection

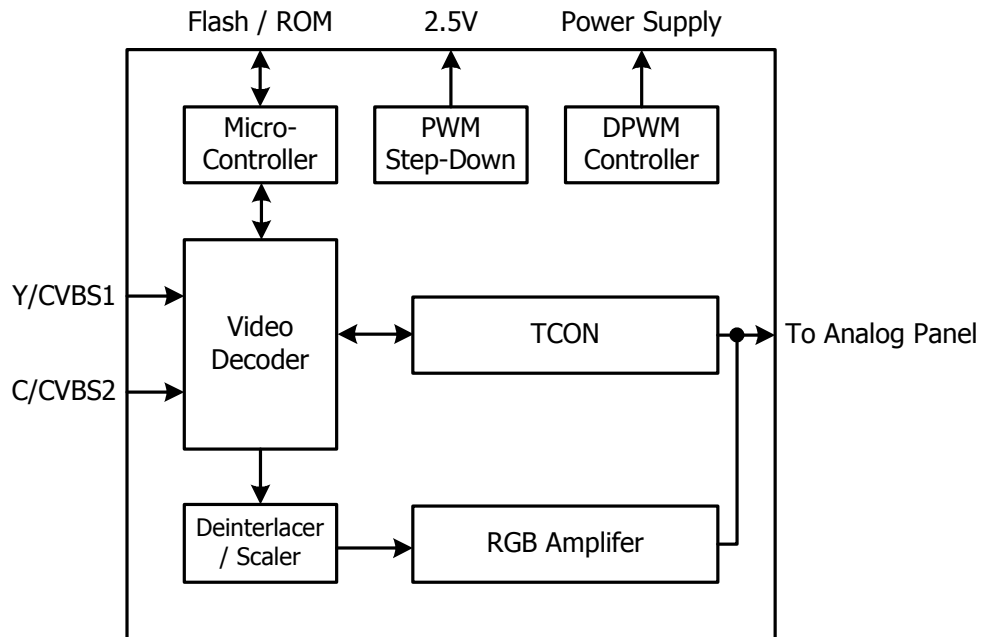
### ■ Miscellaneous

- Built-in MCU
- 3-wire serial bus interface for configuration setup
- Built-in step-down PWM circuits for input 2.5V
- Built-in VCOM DC level adjusting circuits
- Built-in internal OSD with 256 programmable fonts, 16-color palettes, and 12-bit color resolution
- 3-channel low-power 8-bit DAC integration for RGB output, dynamic range 0.1-4.9V
- Built-in VCOM DC/AC level adjustment circuit
- Spread spectrum clocks
- Optional 3.3V / 5V output pads with programmable driving current
- 100-pin LQFP package

**BLOCK DIAGRAM**



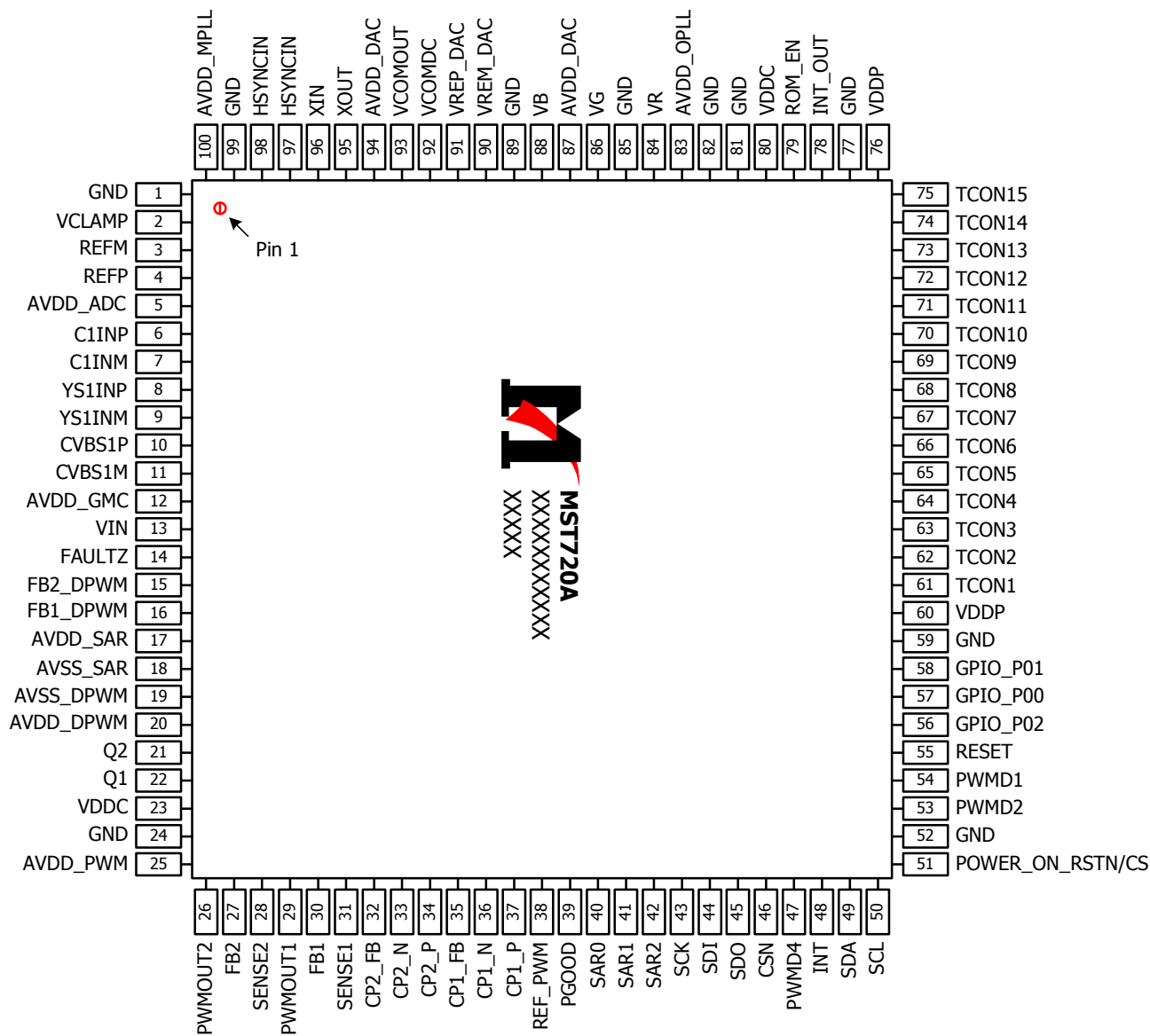
**SYSTEM APPLICATION DIAGRAM**



## GENERAL DESCRIPTION

The MST720A is a high quality ASIC for NTSC/PAL car TV application. It receives analog NTSC/PAL CVBS and S-Video inputs from TV tuners, DVD or VCR sources, including weak and distorted signals. Automatic gain control (AGC) and 8-bit 3-channel A/D converters provide high resolution video quantization. With automatic video source and mode detection, users can easily switch and adjust variety of signal sources. Multiple internal adaptive PLLs precisely extract pixel clock from video source and perform sharp color demodulation. Built-in line-buffer supports adaptive 2-D comb-filter, 2-D sharpening, and synchronization stabler in a condense manner. The output format of MST720A supports 3.5"~7" analog TFT-LCD modules.

**PIN DIAGRAM (MST720A)**



## PIN DESCRIPTION

### Analog Interface

Pin Name	Pin Type	Function	Pin
VCLAMP		CVBS/YC Mode Clamp Voltage Bypass	2
REFM		Internal ADC Bottom De-coupling Pin	3
REFP		Internal ADC Top De-coupling Pin	4
C1INP	Analog Input	Analog Chroma Input for TV S-Video1 / Analog Composite Input of TV CVBS4	6
C1INM	Analog Input	Reference Ground for Analog Chroma Input of TV S-Video1 / Analog Composite Input of TV CVBS4	7
YS1INP	Analog Input	Analog Luma Input of TV S-Video1 / Analog Composite Input of TV CVBS3	8
YS1INM	Analog Input	Reference Ground for Analog Luma Input of TV S-Video1 / Analog Composite Input of TV CVBS3	9
CVBS1P	Analog Input	Analog Composite Input for TV CVBS1	10
CVBS1M	Analog Input	Reference Ground for Analog Composite Input of TV CVBS1	11
HSYNCIN	Schmitt Trigger Input w/ 5V-tolerant	HSYNC / Composite Sync for VGA Input	98
VSYNCIN	Schmitt Trigger Input w/ 5V-tolerant	VSYNC for VGA Input	97

### Analog Panel Output Interface

Pin Name	Pin Type	Function	Pin
VR	Analog Output	Red Channel Output 4.0 Vp-p	84
VG	Analog Output	Green Channel Output 4.0 Vp-p	86
VB	Analog Output	Blue Channel Output 4.0 Vp-p	88
REFM_DAC		DAC Bottom Reference Voltage Decoupling Cap. 1uF to Ground	90
REFP_DAC		DAC Top Reference Voltage Decoupling Cap. 1uF to Ground	91
TCON[15:1]	Output	TCON Output	75-61

### VCOM Interface

Pin Name	Pin Type	Function	Pin
VCOMDC	Analog Output	Reference DC Voltage Output for Common Amplifier	92
VCOMOUT	Analog Output	Pulse Output for Common Voltage.	93

### Switching Power and PWM Interface

Pin Name	Pin Type	Function	Pin
PWMOUT2	Output	Switching Pulse Output for DC-DC Converter	26
FB2	Analog Input	Error Voltage Feedback Input Pin for PWM2; voltage = 1.2V	27
SENSE2	Analog Input	Sense Circuit Connection for PWM2	28
PWMOUT1	Output	Switching Pulse Output for DC-DC Converter	29
FB1	Analog Input	Error Voltage Feedback Input Pin for PWM1; voltage = 1.2V	30
SENSE1	Analog Input	Sense Circuit Connection for PWM1	31
CP2_FB	Analog Input	Error Voltage Feedback Input Pin for CP2; voltage = 1.2V	32
CP2_N	Output	Charge Pump Negative Pulse for DC-DC Negative Voltage Converter	33
CP2_P	Output	Charge Pump Positive Pulse for DC-DC Negative Voltage Converter	34
CP1_FB	Analog Input	Error Voltage Feedback Input Pin for CP1; voltage = 1.2V	35
CP1_N	Output	Charge Pump Negative Pulse for DC-DC Negative Voltage Converter	36
CP1_P	Output	Charge Pump Positive Pulse for DC-DC Negative Voltage Converter	37
REF_PWM		PWM Reference; voltage = 2.4V	38
PGOOD	Output	Power Good Detector	39

### Internal MCU Interface with Serial Flash Memory

Pin Name	Pin Type	Function	Pin
SAR2	Analog Input	SAR Low Speed ADC Input 2	42
SAR1	Analog Input	SAR Low Speed ADC Input 1	41
SAR0	Analog Input	SAR Low Speed ADC Input 0	40
SCK	Output	SPI Interface Sampling Clock	43
SDI	Output	SPI Interface Data-In	44
SDO	Input w/ 5V-tolerant	SPI Interface Data-Out	45
CSN	Output	SPI Interface Chip Select	46
GPIO_P00	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	57
GPIO_P01	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	58
GPIO_P05	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	56
INT	Input	Interrupt Input for IR Receiver	48
SDA	I/O w/ 5V-tolerant	3-Wire Serial Bus Data	49

Pin Name	Pin Type	Function	Pin
SCL	Input w/ 5V-tolerant	3-Wire Serial Bus Clock	50
POWER_ON_RSTN/CS	Input w/ 5V-tolerant	Power On Reset Signal / Chip Selection for 3-wire Serial	51

### Digital PWM Interface

Pin Name	Pin Type	Function	Pin
Q1	Output	DPWM Output 1	22
Q2	Output	DPWM Output 2	21
FB1_DPWM	Analog Input	Input for 1 <sup>st</sup> Feedback Loop	16
FB2_DPWM	Analog Input	Input for 2 <sup>nd</sup> Feedback Loop	15
FAULTZ	Analog Input	Fault Detection (Low Enable)	14
VIN	Analog Input	System Input Voltage Detection	13

### Misc. Interface

Pin Name	Pin Type	Function	Pin
RESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware Reset; active high	55
XIN	Analog Input	Crystal Oscillator Input	96
XOUT	Analog Output	Crystal Oscillator Output	95
PWMD4	Output	Pulse Width Modulation Output; 4mA driving strength	47
PWMD2	Output	Pulse Width Modulation Output; 4mA driving strength	53
PWMD1	Output	Pulse Width Modulation Output; 4mA driving strength	54
INT_OUT	Output	Mode Detection Interrupt Output	78
ROM_EN	Input	Internal ROM Enable. 0: Disable. 1: Enable.	79

### Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_ADC	2.5V Power	ADC Power	5
AVDD_GMC	5V Power	GMC Power	12
AVDD_SAR	2.5V/5V Power	SAR Power	17
AVDD_DPWM	5V Power	DPWM Power	20
AVDD_PWM	5V Power	PWM Power	25
AVDD_OPLL	2.5V Power	OPLL Power	83
AVDD_DAC	5V Power	Voltage DAC Power	87, 94

Pin Name	Pin Type	Function	Pin
AVDD_MPLL	2.5V Power	MPLL Power	100
VDDC	2.5V Power	Digital Core Power	23, 80
VDDP	3.3V/5V Power	Digital Input/Output Power	60, 76
AVSS_SAR	Ground	SAR Ground	18
AVSS_DPWM	Ground	DPWM Ground	19
GND	Ground	Ground	1, 24, 52, 59, 81, 82, 85, 89, 99



## ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
5.0V Supply Voltages	$V_{VDD\_50}$	-0.3		5.5	V
3.3V Supply Voltages	$V_{VDD\_33}$	-0.3		3.6	V
2.5V Supply Voltages	$V_{VDD\_25}$	-0.3		2.75	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$	-0.3		5.0	V
Input Voltage (non 5V tolerant inputs)	$V_{IN}$	-0.3		$V_{VDD\_33}$	V
Ambient Operating Temperature (commercial use)	$T_A$	0		70	°C
Ambient Operating Temperature (extended temp. range)	$T_A$	-20		80	°C
Storage Temperature	$T_{STG}$	-40		125	°C
Operating Junction Temperature	$T_J$	0		125	°C
Thermal Resistance (Junction to Air) Natural Convection	$\theta_{JA}$		TBD		°C/W
Thermal Resistance (Junction to Case) Natural Convection	$\theta_{JC}$		TBD		°C/W

**Note: Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.**

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MST720A	0°C to +70°C	LQFP	100
MST720A-A	-20°C to +80°C	LQFP	100
MST720A-LF	0°C to +70°C	LQFP	100
MST720A-A-LF	-20°C to +80°C	LQFP	100

**Note: Product suffix "-LF" represents lead-free version and "-A" represents extended temperature range.**

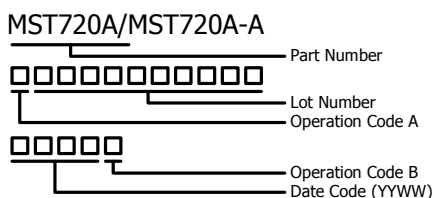
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**Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST720A comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.**

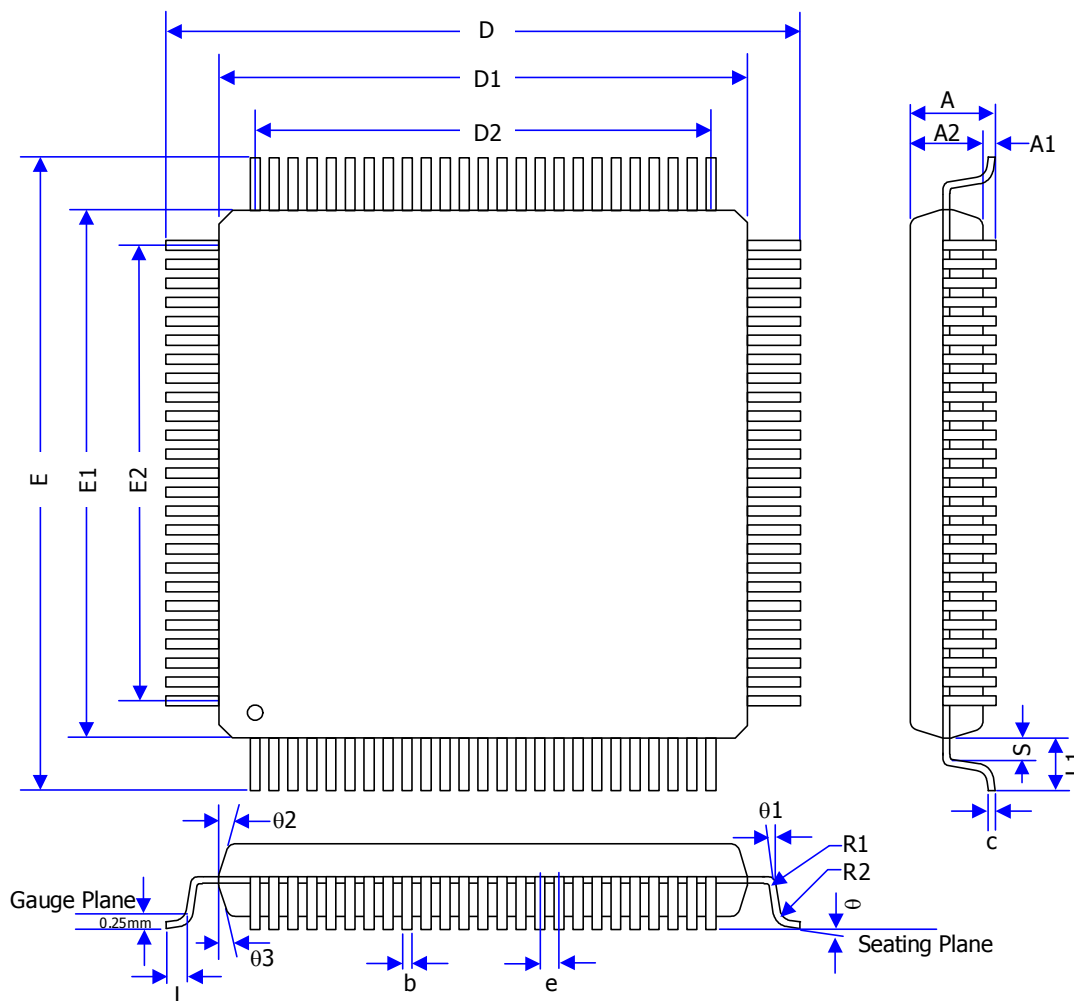
## MARKING INFORMATION



**REVISION HISTORY**

<b>Document</b>	<b>Description</b>	<b>Date</b>
MST720A_ds_v01	<ul style="list-style-type: none"><li>• Initial release</li></ul>	Nov 2005
MST720A_ds_v02	<ul style="list-style-type: none"><li>• Updated Pin Description \ Power Pins</li></ul>	Feb 2006
MST720A_ds_v03	<ul style="list-style-type: none"><li>• Updated Features \ Video Decoder</li><li>• Updated General Description</li><li>• Updated Register Table</li></ul>	Mar 2006

## MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
D2	12.00			0.472		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
E2	12.00			0.472		
R1	0.08	-	-	0.003	-	-
R2	0.08	-	0.20	0.003	-	0.008

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
$\theta$	0°	3.5°	7°	0°	3.5°	7°
$\theta 1$	0°	-	-	0°	-	-
$\theta 2$	11°	12°	13°	11°	12°	13°
$\theta 3$	11°	12°	13°	11°	12°	13°
b	0.17	0.20	0.27	0.007	0.008	0.011
c	0.09	-	0.20	0.004	-	0.008
e	0.50 BSC.			0.020 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 Ref			0.039 Ref		
S	0.20	-	-	0.008	-	-

## REGISTER DESCRIPTION

### General Control Register

General Control Register				
Index	Name	Bits	Description	
00h	<b>REGBK</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	XTAL_OK (RO)	7	Crystal ready.	
	MCU_SEL (RO)	6	0: Embedded MCU. 1: External serial bus interface.	
	-	5:4	Reserved.	
	AINC	3	Serial bus address auto Increase. 0: Enable. 1: Disable.	
	REGBK[2:0]	2:0	Register Bank Select. 000: Register of scaler. 001: Register of ADC/ACE/MCU. 010: Register of Video Decoder Front End (VFE). 011: Register of Video Decoder 2D Comb Filter (VCF). 100: Register of DPWM.	
01h ~ FFh	-	7:0	<b>Default : -</b>	<b>Access : -</b>
	-	7:0	Reserved.	

### Scaler Register (Bank = 00, Registers 01h ~ 9Fh)

Scaler Register (Bank=00, Registers 01h ~ 9Fh)				
Index	Name	Bits	Description	
01h	<b>DBFC</b>	<b>7:0</b>	<b>Default : 0x80</b>	<b>Access : R/W</b>
	-	7:3	Reserved.	
	DBL[1:0]	2:1	Double Buffer Load. 00: Keep old register value. 01: Load new data (auto reset to 00 when load finish). 10: Automatically load data at VSYNC blanking. 11: Reserved.	
	DB_EN	0	Double Buffer Enable. 0: Disable. 1: Enable.	
02h	<b>ISELECT</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	NIS	7	No Input Source. 0: Input source active. 1: Input source inactive, output is free-run.	

### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
	STYPE[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).
	COMP	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.
	ICS	3	Input Color Space. 0: RGB. 1: YCbCr.
	IHSU	2	Input Sync Usage. When EXTVD=0: 0: Use HSYNC to perform mode detection, HSOUT from ADC to sample pixel. 1: Use HSYNC only. When EXTVD=1: 0: Normal. 1: Output black at blanking.
	BYPASSMD	1	By-Pass Mode for interlace-input-interlace-output.
	EXTVD	0	0: Select analog input (CVBS/S-Video/RGB/YCbCr). 1: Select digital input (CCIR656).
<b>03h</b>	<b>IPCTRL2</b>	<b>7:0</b>	<b>Default : 0x18</b> <b>Access : R/W</b>
	VDS_EN	7	Input data double sample In CCIR input mode, 0: for horizontal output resolution less than 720 pixels. 1: for horizontal output resolution more than 720 pixels. In analog input mode, 0: half sample of input data. 1: original sample of input data.
	VDS_MTHD	6	Input data double sample Method. 0: Using average. 1: Using advance GT filter.
	IVDS	5	Input VSYNC Delay Select. 0: Delay 1/4 input HSYNC (recommended). 1: No delay.
	HES	4	Input HSYNC reference Edge Select. 0: From HSYNC leading edge, default value. 1: From HSYNC tailing edge.

### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
	VES	3	Input VSYNC reference Edge Select. 0: From VSYNC leading edge, default value. 1: From VSYNC tailing edge.
	ESLS	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.
	VWRP	1	Input image Vertical Wrap. 0: Disable. 1: Enable.
	HWRP	0	Input image Horizontal Wrap. 0: Disable. 1: Enable.
<b>04h</b>	<b>ISCTRL</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>
	DDE	7	Direct DE mode for CCIR input. 0: Disable direct DE. 1: Enable direct DE.
	DEGR[2:0]	6:4	DE or HSYNC post Glitch removal Range.
	HSFL	3	Input HSYNC Filter. 0: Filter off. 1: Filter on.
	ISSM	2	Input Sync Sample Mode. 0: Normal. 1: Glitch-removal.
	MVD_SEL	1:0	MVD mode Select 0: CVBS. 1: S-Video. 2: YCbCr. 3: RGB.
<b>05h</b>	<b>SPRVST_L</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W, DB</b>
	SPRVST[7:0]	7:0	Image vertical sample start point, count by input HSYNC (lower 8 bits).
<b>06h</b>	<b>SPRVST_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W, DB</b>
	-	7:3	Reserved.
	SPRVST[10:8]	2:0	Image vertical sample start point, count by input HSYNC (higher 3 bits).
<b>07h</b>	<b>SPRHST_L</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W, DB</b>

### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
	SPRHST[7:0]	7:0	Image horizontal sample start point, count by input dot clock (higher 8 bits).
<b>08h</b>	<b>SPRHST_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W, DB</b></span>
	-	7:3	Reserved.
	SPRGST[10:8]	2:0	Image horizontal sample start point, count by input dot clock (lower 3 bits).
<b>09h</b>	<b>SPRVDC_L</b>	<b>7:0</b>	<b>Default : 0x10</b> <span style="float: right;"><b>Access : R/W, DB</b></span>
	SPRVDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line; lower 8 bits).
<b>0Ah</b>	<b>SPRVDC_H</b>	<b>7:0</b>	<b>Default: 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	-	7:3	Reserved.
	SPRVDC[10:8]	2:0	Image vertical resolution (vertical display enable area count by line; higher 3 bits).
<b>0Bh</b>	<b>SPRHDC_L</b>	<b>7:0</b>	<b>Default : 0x10</b> <span style="float: right;"><b>Access : R/W</b></span>
	SPRHDC[7:0]	7:0	Image horizontal resolution (horizontal display enable area count by pixel; lower 8 bits).
<b>0Ch</b>	<b>SPRHDC_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	-	7:3	Reserved.
	SPRHDC[10:8]	2:0	Image horizontal resolution (horizontal display enable area count by pixel; higher 3 bits).
<b>0Dh</b>	<b>LYL</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	-	7:4	Reserved.
	LYL[3:0]	3:0	Lock Y Line.
<b>0Eh</b>	<b>INTLX</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : -</b></span>
	ITU_EXT_FIELD	7	Using External FIELD for ITU interface. 0: Using EAV/SAV. 1: Using external FIELD.
	ITU_EXT_HS	6	Using External HSYNC for ITU interface. 0: Using EAV/SAV. 1: Using external HSYNC.
	ITU_EXT_VS	5	Using External VSYNC for ITU interface. 0: Using EAV/SAV. 1: Using external VSYNC.
	VDOE	4	Video reference Edge (for non-standard signal).
	INTLAC_LOCKAVG	3	Averaging Locking timing.

### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
	LHC_MD	2	Long Horizontal Counter Mode. 1: On. 0: Off.
	-	1:0	Reserved.
<b>0Fh</b>	<b>ASCTRL</b>	<b>7:0</b>	<b>Default : 0x90</b> <b>Access : R/W</b>
	IVB (RO)	7	Input VSYNC Blanking status. 0: In display. 1: In blanking.
	DLINE[2:0]	6:4	Line buffer read delay in number of lines.
	INTLAC_MANSTD	3	NTSC/PAL Manual Mode
	INTLAC_SETSTD	2	NTSC/PAL Setting in manual mode under run status. 0: NTSC. 1: PAL.
	UNDER (RO)	1	Under run status.
	OVER (RO)	0	Over run status.
<b>10h</b>	<b>COCTRL1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	AVI_SEL	5	Analog Video Input Select. 0: PC. 1: Component analog video.
	DLYV	4	Analog Delay line for component analog Video input. 0: Delay 1 line. 1: Do not delay.
	CSC_MD	3	Composite SYNC Cut Mode. 0: Disable. 1: Enable.
	EXVS	2	External VSYNC polarity (only used when COVS is 1). 0: Normal. 1: Invert.
	COV_SEL	1	Coast VSYNC Select. 0: Internal VSEP. 1: External VSYNC.
	CADC	0	Coast to ADC. 0: Disable. 1: Enable.
<b>11h</b>	<b>COCTRL2</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>



### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
	COST[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. ... 254: Coast start from 255 HSYNC leading edge. 255: Coast start from 256 HSYNC leading edge.
12h	<b>COCTRL3</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	COEND[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. ... 254: Coast end at 255 HSYNC leading edge. 255: Coast end at 256 HSYNC leading edge.
13h	<b>VFAC_OINI</b>	<b>7:0</b>	<b>Default: 0x00</b> <b>Access : R/W</b>
	VFACOINI[7:0]	7:0	Vertical Factor Odd Initial value.
14h	<b>VFAC_EINI</b>	<b>7:0</b>	<b>Default: 0x80</b> <b>Access : R/W</b>
	VFACEINI[7:0]	7:0	Vertical Factor Even Initial value
15h	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
16h	<b>INTCTROL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CHG_HMD	7	Change H Mode for INT. 0: Only in leading/tailing of CHG period. 1: Every line generating INT pulse during CHG period.
	-	6:4	Reserved.
	IVSI	3	Input VSYNC interrupt generated by: 0: Leading edge. 1: Tailing edge.
	OVSI	2	Output VSYNC interrupt generated by: 0: Leading edge. 1: Tailing edge.
	TRGC	1	Trigger Condition. 0: Active low for level trigger/tailing edge trigger. 1: Active high for level trigger/leading edge trigger.
	INT_TRIG	0	Interrupt Trigger. 0: Generate an edge trigger interrupt. 1: Generate a level trigger interrupt.
17h	<b>INTPULSE</b>	<b>7:0</b>	<b>Default : 0x0F</b> <b>Access : R/W</b>

### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
	INTPULSE[7:0]	7:0	Interrupt Pulse width by reference clock.
18h	<b>INTSTA</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	INTSTA[7:0]	7:0	Interrupt Status byte A. Bit 7: MVD input NOT "no signal". Bit 6: MVD "HSYNC lock". Bit 5: MVD NOT "no color". Bit 4: MVD degree error. Bit 3: MVD input "no signal". Bit 2: MVD NOT "HSYNC lock". Bit 1: MVD "no color". Bit 0: MVD HSYNC change.
19h	<b>INTENA</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	INTENA[7:0]	7:0	Interrupt Enable control byte A. 0: Disable interrupt. 1: Enable interrupt.
1Ah	<b>INTSTB</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	INTSTB[7:0]	7:0	Interrupt Status byte B. Bit 7: MCU D2B interrupt 2. Bit 6: MCU D2B interrupt 1. Bit 5: MCU D2B interrupt 0. Bit 4: MVD CC interrupt. Bit 3: Reserved. Bit 2: MVD PAL switch error. Bit 1: MVD "ADC7_0ACT". Bit 0: MVD NOT "ADC7_0ACT".
1Bh	<b>INTENB</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/C</b>
	INTENB[7:0]	7:0	Interrupt Enable control byte B. 0: Disable interrupt. 1: Enable interrupt.
1Ch	<b>INTSTC</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	INTSTC[7:0]	7:0	Interrupt Status byte C. Bit 7: Output VSYNC interrupt. Bit 6: Input VSYNC interrupt. Bit 5: ATG ready interrupt. Bit 4: ATP ready interrupt. Bit 3: ATS ready interrupt. Bit 2: MVD probe ready interrupt. Bit 1: MCU D2B interrupt 4. Bit 0: MCU D2B interrupt 3.

**Scaler Register (Bank=00, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
1Dh	<b>INTENC</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/C</b>
	INTENC[7:0]	7:0	Interrupt Enable control byte C. 0: Disable interrupt. 1: Enable interrupt.
1Eh	<b>INTSTD</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	INTSTD[7:0]	7:0	Interrupt Status byte D. Bit 7: WDT interrupt. Bit 6: Keypad wake-up interrupt. Bit 5: Jitter interrupt. Bit 4: Horizontal total change interrupt. Bit 3: Vertical total change interrupt. Bit 2: Horizontal lost count interrupt. Bit 1: Vertical lost count interrupt. Bit 0: Standard change interrupt.
1Fh	<b>INTEND</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/C</b>
	INTEND[7:0]	7:0	Interrupt Enable control byte D. 0: Disable interrupt. 1: Enable interrupt.
20h ~ 21h	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
22h	<b>MPL_M</b>	<b>7:0</b>	<b>Default : 0x6F</b> <b>Access : R/W</b>
	MP_ICTRL[2:0]	7:5	Charge pump current set.
	MPL_M[4:0]	4:0	MPLL divider ratio setting.
23h	<b>OPL_CTL0</b>	<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	SSC_EN	6	Output PLL spread spectrum. 0: Disable. 1: Enable.
	SD_MD	5	Output PLL spread spectrum Mode. 0: Normal. 1: Reverse for mode 1.
	-	4:0	Reserved.
24h	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
25h	<b>OPL_SET0</b>	<b>7:0</b>	<b>Default : 0x44</b> <b>Access : R/W, DB</b>
	OPL_SET[7:0]	7:0	Output PLL Set.

### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
26h	<b>OPL_SET1</b>	<b>7:0</b>	<b>Default : 0x55</b> <b>Access : R/W, DB</b>
	OPL_SET[15:8]	7:0	See description for OPL_SET [7:0].
27h	<b>OPL_SET2</b>	<b>7:0</b>	<b>Default : 0x24</b> <b>Access : R/W, DB</b>
	OPL_SET [23:16]	7:0	See description for OPL_SET [7:0].
28h	<b>OPL_STEP0</b>	<b>7:0</b>	<b>Default : 0x20</b> <b>Access : R/W, DB</b>
	OPL_STEP[7:0]	7:0	Output PLL spread spectrum Step.
29h	<b>OPL_STEP1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W, DB</b>
	-	7	Reserved.
	-	6	Reserved.
	-	5	Reserved.
	-	4:3	Reserved.
	OPL_STEP[10:8]	2:0	See description for OPL_STEP[7:0].
2Ah	<b>OPL_SPAN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W, DB</b>
	OPL_SPAN[7:0]	7:0	Output PLL spread spectrum Span.
2Bh	<b>OPL_SPAN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W, DB</b>
	READ_FRAME	7	0: OPL_SET stores line-based value. 1: OPL_SET stores frame-based value.
	OPL_SPAN[14:8]	6:0	See description for OPL_SPAN[7:0].
2Ch ~ 2Fh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
30h	<b>HSR_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	HSR [7:0]	7:0	Horizontal Scaling ratio (20 bits fraction) for scaling down $1/2^{20}$ to $(2^{20}-1)/2^{20}$ (lower 8 bits).
31h	<b>HSR_M</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	HSR[15:8]	7:0	Horizontal Scaling ratio (20 bits fraction) for scaling down $1/2^{20}$ to $(2^{20}-1)/2^{20}$ (middle 8 bits).
32h	<b>HSR_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	HS_EN	7	Horizontal Scaling Enable. 0: Disable. 1: Enable.
	CBILINEAR_EN	6	Complemental Bi-Linear Enable.
	FORCEBICOLOR	5	0: Chrominance using same setting as Luminance defined by CBILINEAR. 1: Chrominance always using bi-linear algorithm.

<b>Scaler Register (Bank=00, Registers 01h ~ 9Fh)</b>				
<b>Index</b>	<b>Name</b>	<b>Bits</b>	<b>Description</b>	
	-	4	Reserved.	
	HSR[19:16]	3:0	Horizontal Scaling Ratio (20 bits fraction) for scaling down $1/2^{20}$ to $(2^{20}-1)/2^{20}$ (higher 8 bits).	
<b>33h</b>	<b>VSR_L</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	VSR[7:0]	7:0	Vertical Scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999 (lower 8 bits). xx.xxxxxxxxxxxxxxxxxxxxxx	
<b>34h</b>	<b>VSR_M</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	VSR[15:8]	7:0	Vertical Scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999 (middle 8 bits). xx.xxxxxxxxxxxxxxxxxxxxxx	
<b>35h</b>	<b>VSR_H</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	VS_EN	7	Vertical Scaling Enable. 0: Disable. 1: Enable.	
	VSM_SEL	6	Vertical Scaling Method Select. 0: Original. 1: New.	
	VSR[21:16]	5:0	Vertical Scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999 (higher 8 bits). xx.xxxxxxxxxxxxxxxxxxxxxx	
<b>36h</b>	<b>VDSUSG</b>	<b>7:0</b>	<b>Default: 0x00</b>	<b>Access : R/W</b>
	LBF_INCLK	7	Line-Buffer using Input Clock.	
	LBF_OUTCLK	6	Line-Buffer using Output Clock.	
	LBF_LIVE	5	Line-Buffer always Live.	
	OUTCLK_DIV3	4	Output Clock is 1/3 frequency of OPLL output.	
	EN_OFST	3	Enable Offset for even/odd scaling.	
	OFST_INV	2	Offset Inverting for even/odd scaling.	
	LBCLK_DIV2	1	Line-Buffer Clock frequency is divided by 2.	
	VSD_DITH_EN	0	VSD Dither Enable.	
<b>37h</b>	<b>DIRSCAL_CTL</b>	<b>7:0</b>	<b>Default: 0x00</b>	<b>Access : R/W</b>
	-	7:3	Reserved.	
	GOAL2_SEL	2	Goal2 Select.	
	DITH_ON	1	Dithering control. 0: Off. 1: On.	

**Scaler Register (Bank=00, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	DIRSCAL_EN	0	Function Enable.
38h	<b>NLDTI</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	NL_EN	7	Non-Linear scaling Enable.
	NLSIO[6:0]	6:0	Non-Linear Scaling section Initial Offset.
39h	<b>NLDT0</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	NLIOS	7	Non-Linear scaling section Initial Offset Sign. 0: Positive value. 1: Negative value.
	NLDT0[6:0]	6:0	Non-Linear Scaling Delta for Section 0, bit 7 is sign bit.
3Ah	<b>NLDT1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved
	NLDT1[6:0]	6:0	Non-Linear scaling Delta for Section 1, bit 7 is sign bit.
3Bh	<b>NLDC0</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	NLDC0[7:0]	7:0	Non-Linear scaling section 0 Dot Count/2.
3Ch	<b>NLDC1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	NLDC1[7:0]	7:0	Non-Linear scaling section 1 Dot Count/2.
3Dh	<b>NLDC2</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	NLDC2[7:0]	7:0	Non-Linear scaling section 2 Dot Count/2.
3Eh	<b>DIRSCAL_TH1</b>	<b>7:0</b>	<b>Default: 0x80</b> <b>Access : R/W</b>
	DETH[7:0]	7:0	Threshold of maximum value for detection
3Fh	<b>DIRSCAL_TH2</b>	<b>7:0</b>	<b>Default: 0x80</b> <b>Access : R/W</b>
	PCTTH[7:0]	7:0	Threshold of maximum value for protection
40h	<b>VFDEST_L</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	VFDEST[7:0]	7:0	Output frame DE Vertical Start (lower 8 bits).
41h	<b>DEVST_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	VFDEST[10:8]	2:0	Output frame DE Vertical Start (higher 3 bits).
42h	<b>HFDEST_L</b>	<b>7:0</b>	<b>Default : 0x03</b> <b>Access : R/W</b>
	HFDEST[7:0]	7:0	Output frame DE Horizontal Start (lower 8 bits).
43h	<b>HFDEST_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	HFDEST[10:8]	2:0	Output frame DE Horizontal Start (higher 3 bits).
44h	<b>VFDEEND_L</b>	<b>7:0</b>	<b>Default : 0xEA</b> <b>Access : R/W</b>

### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
	VFDEEND[7:0]	7:0	Output frame DE Vertical END (lower 8 bits).
45h	<b>VFDEEND_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	DEVEND[10:8]	2:0	Output frame DE Vertical END (higher 3 bits).
46h	<b>HFDEEND_L</b>	<b>7:0</b>	<b>Default : 0xE0</b> <b>Access : R/W</b>
	HFDEEND[7:0]	7:0	Output frame DE Horizontal END (lower 8 bits).
47h	<b>HFDEEND_H</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	HFDEEND[10:8]	2:0	Output frame DE Horizontal END (higher 3 bits).
48h	<b>SIHST_L</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start (lower 8 bits).
49h	<b>SIHST_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	SIHST[10:8]	2:0	Scaling Image window Horizontal Start (higher 3 bits).
4Ah	<b>SIVEND_L</b>	<b>7:0</b>	<b>Default : 0xEA</b> <b>Access : R/W</b>
	SIVEND[7:0]	7:0	Scaling Image window Vertical END (lower 8 bits).
4Bh	<b>SIVEND_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	SIVEND[10:8]	2:0	Scaling Image window Vertical END (higher 3 bits).
4Ch	<b>SIHEND_L</b>	<b>7:0</b>	<b>Default : 0xEA</b> <b>Access : R/W</b>
	SIHEND[7:0]	7:0	Scaling Image window Horizontal END (lower 8 bits).
4Dh	<b>SIHEND_H</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	SIHEND[10:8]	2:0	Scaling Image window Horizontal END (higher 3 bits).
4Eh	<b>VDTOT_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	VDTOT[7:0]	7:0	Output Vertical Total (lower 8 bits).
4Fh	<b>VDTOT_H</b>	<b>7:0</b>	<b>Default : 0x02</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	VDTOT[10:8]	2:0	Output Vertical Total (higher 3 bits).
50h	<b>VSST_L</b>	<b>7:0</b>	<b>Default : 0xEA</b> <b>Access : R/W</b>
	VSST[7:0]	7:0	Output VSYNC start (lower 8 bits).
51h	<b>VSST_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:4	Reserved.

**Scaler Register (Bank=00, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	VSRU	3	VSYNC Register Usage. 0: Registers 20h – 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No signal VSYNC. Registers 22h and 23h are used to define minimum H total.
	VSST[10:8]	2:0	Output VSYNC start (higher 3 bits).
52h	<b>VSEND_L</b>	<b>7:0</b>	<b>Default : 0x06</b> <b>Access : R/W</b>
	VSEND[7:0]	7:0	Output VSYNC END (lower 8 bits).
53h	<b>VSEND_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W DB</b>
	-	7:3	Reserved.
	VSEND[10:8]	2:0	Output VSYNC END (higher 3 bits).
54h	<b>HDTOT_L</b>	<b>7:0</b>	<b>Default : 0x3C</b> <b>Access : R/W DB</b>
	HDTOT[7:0]	7:0	Output Horizontal Total (lower 8 bits).
55h	<b>HDTOT_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	HDTOT[10:8]	2:0	Output Horizontal Total (higher 3 bits).
56h	<b>HSEND</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	HSEND[7:0]	7:0	Output HSYNC END (lower 8 bits).
57h	<b>OSCTRL1</b>	<b>7:0</b>	<b>Default : 0x4C</b> <b>Access : R/W</b>
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x50 – 0x53).
	LCM	6	Frame Lock Mode. 0: Mode 0. 1: Mode 1.
	HRSM	5	HSYNC Remove Mode. 0: Normal. 1: Remove HSYNC.
	-	4:3	Reserved.
	Scal_1	2	Scaling range add 1.
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.
58h	<b>BRIGHTNESS_EN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>



### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
	-	7:1	Reserved.
	BRI_EN	0	Brightness function Enable. 0: Disable. 1: Enable.
59h	<b>BRI_R</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	BRI_R[7:0]	7:0	Brightness coefficient–Red color.
5Ah	<b>BRI_G</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	BRI_G[7:0]	7:0	Brightness coefficient–Green color.
5Bh	<b>BRI_B</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	BRI_B[7:0]	7:0	Brightness coefficient–Blue color.
5Ch	<b>FRAME_COLOR_1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	FCG[4:3]	7:6	Frame Color G[4:3].
	FCB[7:3]	5:1	Frame Color B[7:3].
	FC_EN	0	Frame Color Enable. 0: Diable. 1: Enable.
5Dh	<b>FRAME_COLOR_2</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	FCR[7:3]	7:3	Frame Color R[7:3].
	FCG[7:5]	2:0	Frame Color G[7:5].
5Eh	<b>PATTERN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EXT_OSD	7	EXT OSD pin as GPIO.
	EXT_VD	6	EXT VD pin as GPIO.
	-	5:3	Reserved.
	PTNWT	2	Pattern White.
	PTNBLK	1	Pattern Black.
	PTNRVS	0	Pattern Reverse.
5Fh	<b>EXT_OSD_CTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EXTOSD_EN	7	External OSD function Enable. 0: Diable. 1: Enable.
	DATEXTMD[1:0]	6:5	Data Extend Mode.
	CKEY_EN	4	Color Key Enable. 0: Disable. 1: Enable.

**Scaler Register (Bank=00, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	INVCKEY_EN	3	Inverse Color Key Enable. 0: Disable. 1: Enable.
	R_KEY	2	R color Key selected.
	G_KEY	1	G color Key selected.
	B_KEY	0	B color Key selected.
<b>60h</b>	<b>DITHCTRL</b>	<b>7:0</b>	<b>Default : 0x02</b> <b>Access : R/W</b>
	DITHG[1:0]	7:6	Dither coefficient for G channel.
	DITHB[1:0]	5:4	Dither coefficient for B channel.
	SROT	3	Spatial coefficient Rotate. 0: Disable. 1: Enable.
	TROT	2	Temporal coefficient Rotate. 0: Disable. 1: Enable.
	OBN	1	Output Bits Number 0: 8-bit output. 1: 6-bit output (power on default value).
	DITH	0	Dither function. 0: Off. 1: On.
<b>61h</b>	<b>DITHCOEF</b>	<b>7:0</b>	<b>Default : 0x2D</b> <b>Access : R/W</b>
	TL[1:0]	7:6	Top-Left dither coefficient.
	TR[1:0]	5:4	Top-Right dither coefficient.
	BL[1:0]	3:2	Bottom-Left dither coefficient.
	BR[1:0]	1:0	Bottom-Right dither coefficient.
<b>62h</b>	<b>DITHCTL1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	PSRD	7	Pseudo Random, resets every 4 frames. 0: Enable. 1: Disable.
	ND_MD	6	Noise Dithering Method.
	AUTO_DTH	5	Auto Dither.
	PSDO_EN	4	Pseudo Enable. 0: Disable. 1: Enable.

**Scaler Register (Bank=00, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	DTH_MNUS	3	Dither Minus.
	ABM[2:0]	2:0	Alpha Blending Mode. 000: No alpha blending. 001: Background alpha blending. 010: Foreground alpha blending. 011: Color key alpha blending. 100: Not color key alpha blending. 101: Entire OSD alpha blending. 11x: Reserved.
<b>63h</b>	<b>OSD_CTL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CKIND[3:0]	7:4	Color Index of Color Key. 0000: Color index 0. 0001: Color index 1. ... .. 1111: Color index 15. When OSD register 0x10[7]=1, OSD is not backward compatible. When OSD register 0x10[7]=0, OSD is backward compatible. When 8-color palette is selected, only CKIND[2:0] are used. When 16-color palette is selected, OSD0xE0 bit[6] is color key bit[3] instead of using CKIND[3].
	NEW_BLND_MTHD	3	New Blending Level. 0: Original blending level (BLENDL=000 means 0% transparency). 1: New blending level (BLENDL=000 means 12.5% transparency).
	OSD_BLND_MD	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0%% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.
<b>64h</b>	<b>CM11_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CM11[7:0]	7:0	Color Matrix Coefficient 11 (lower 8 bits).
<b>65h</b>	<b>CM11_H</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	CM11[12:8]	4:0	Color Matrix Coefficient 11 (higher 5 bits).
<b>66h</b>	<b>CM12_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>

**Scaler Register (Bank=00, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	CM12[7:0]	7:0	Color Matrix Coefficient 12 (lower 8 bits).
67h	<b>CM12_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	CM12[12:8]	4:0	Color Matrix Coefficient 12 (higher 5 bits).
68h	<b>CM13_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CM13[7:0]	7:0	Color Matrix Coefficient 13 (lower 8 bits).
69h	<b>CM13_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	CM13[12:8]	4:0	Color Matrix Coefficient 13 (higher 5 bits).
6Ah	<b>CM21_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CM21[7:0]	7:0	Color Matrix Coefficient 21 (lower 8 bits).
6Bh	<b>CM21_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	CM21[12:8]	4:0	Color Matrix Coefficient 21 (higher 5 bits).
6Ch	<b>CM22_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CM22[7:0]	7:0	Color Matrix Coefficient 22 (lower 8 bits).
6Dh	<b>CM22_H</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	CM22[12:8]	4:0	Color Matrix Coefficient 22 (higher 5 bits).
6Eh	<b>CM23_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CM23[7:0]	7:0	Color Matrix Coefficient 23 (lower 8 bits).
6Fh	<b>CM23_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	CM23[12:8]	4:0	Color Matrix Coefficient 23 (higher 5 bits).
70h	<b>CM31_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CM31[7:0]	7:0	Color Matrix Coefficient 31 (lower 8 bits).
71h	<b>CM31_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	CM31[12:8]	4:0	Color Matrix Coefficient 31 (higher 5 bits).
72h	<b>CM32_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CM32[7:0]	7:0	Color Matrix Coefficient 32 (lower 8 bits).
73h	<b>CM32_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.

**Scaler Register (Bank=00, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	CM32[12:8]	4:0	Color Matrix Coefficient 32 (higher 5 bits).
74h	<b>CM33_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CM33[7:0]	7:0	Color Matrix Coefficient 33 (lower 8 bits).
75h	<b>CM33_H</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	CM33[12:8]	4:0	Color Matrix Coefficient 33 (higher 5 bits).
76h	<b>COL_MATRIX_CTL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.
	-	3	Reserved.
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.
77h	<b>FBL_CTL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved
	ODDF	3	Shift Odd Field. 0: Shift even field. 1: Shift odd field.
	SLN[2:0]	2:0	Shift Line Number. 000: Shift 0 line between odd and even fields. 001: Shift 1 line between odd and even fields. 010: Shift 2 line between odd and even fields. 011: Shift 3 line between odd and even fields. 1xx: Shift 4 line between odd and even fields.
78h	<b>LCK_VCNT_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>

**Scaler Register (Bank=00, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	LCK_VCNT[7:0]	7:0	Lock V total low byte [7:0].
79h	<b>LCK_VCNT_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SWCH_STS	7	Switch Status.
	-	6:3	Reserved.
	LCK_VCNT[10:8]	2:0	Lock V total high byte [10:8].
7Ah	<b>CAP_VCNT_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	CAP_VCNT[7:0]	7:0	Cap V total low byte [7:0].
7Bh	<b>CAP_VCNT_H</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-	7:3	Reserved.
	CAP_VCNT[10:8]	2:0	Cap V total high byte [10:8].
7Ch	<b>CAP_HCNT_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	CAP_HCNT[7:0]	7:0	Cap H total low byte [7:0].
7Dh	<b>CAP_HCNT_H</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-	7:3	Reserved.
	CAP_HCNT[10:8]	2:0	Cap H total high byte [10:8].
7Eh	<b>EST_VCNT_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	EST_VCNT[7:0]	7:0	Est V total low byte [7:0].
7Fh	<b>EST_VCNT_H</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-	7:3	Reserved.
	EST_VCNT[10:8]	2:0	Est V total high byte [10:8].
80h	<b>EST_HCNT_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EST_HCNT[7:0]	7:0	Est H total low byte [7:0].
81h	<b>EST_HCNT_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	EST_HCNT[10:8]	2:0	Est H total low byte [10:8].
82h	<b>SSC_TLRN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SSC_TLRN[7:0]	7:0	SSC Tolerance.
83h	<b>Delta_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	DELTA[7:0]	2:0	Delta[7:0].
84h	<b>Delta_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	DELTA[12:8]	4:0	Delta[12:8].
85h	<b>SSC_SHIFT</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>

### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
	SSC_SHIFT[7:0]	7:0	SSC Shift.
<b>86h</b>	<b>FNTN_TST</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	MSK_SHRT_LN_CLK	5	Mask the Clock when in Short Line.
	-	4	Reserved.
	SYNC_GATE_MD	3	Mask HYSNC and Clock Mode.
	RB_SWAP	2	Output channel RB Swap.
	LM_SWAP_6	1	Output Channel MSB LSB Swap in 6-bit bus mode.
	LM_SWAP_8	0	Output Channel MSB LSB Swap in 8-bit bus mode.
<b>87h</b>	<b>DEBUG</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	EOCK	6	Select External ODCLK.
	-	5:4	Reserved.
	PTEN	3	PLL Test register protect bit Enable. 0: Disable. 1: Enable.
	-	2:0	Reserved.
<b>88h</b>	<b>SL_CNTRL_1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	LIM_HS	5	Limit HSYNC period enable.
	-	4:3	Reserved.
	INT_CAP_EN	2	Interlace Capture Enable.
	SHLN_FLD	1	Select Short Line Field.
	FRZ_SHLN	0	Stop Short Line Update.
<b>89h</b>	<b>SL_TUNE_1</b>	<b>7:0</b>	<b>Default : 0x70</b> <b>Access : R/W</b>
	TNCOEF	7:5	Tune Coefficient.
	LCK_THRHD	4:0	Lock Threshold.
<b>8Ah</b>	<b>SL_TUNE_2</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	LMT_D5D6D7_H	7:0	Limit PLL_SET High byte.
<b>8Bh</b>	<b>SL_TUNE_3</b>	<b>7:0</b>	<b>Default : 0xC0</b> <b>Access : R/W</b>
	LMT_D5D6D7_L	7:0	Limit PLL_SET Low byte.
<b>8Ch</b>	<b>TARGET_SL_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	TARGET_SL_L	7:0	Target Short Line Low byte.

### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
8Dh	<b>TARGET_SL_H</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	TARGET_SL_H	7:0	Target Short Line High byte.
8Eh ~ 8Fh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-		Reserved.
90h	<b>GAMMA_EN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:2	Reserved.
	ADR_INC_EN	1	Address Increase Enable. 0: Disable. 1: Enable.
	GAMMA_EN	0	Gamma Enable. 0: Disable. 1: Enable.
91h	<b>GAMMA_ADR_PORT</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	GMA_ADR_PORT[7:0]	7:0	Gamma Address Port [7:0].
92h	<b>GAMMA_DAT_PORT</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	GMA_DAT_PORT[7:0]	7:0	Gamma Data Port [7:0].
93h	<b>R_BIAS</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	R_BIAS[7:0]	7:0	DC level in R channel positive part.
94h	<b>R_RATIO</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	R_RATIO[7:0]	7:0	Ratio in R channel positive part.
95h	<b>G_BIAS</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	G_BIAS[7:0]	7:0	DC level in G channel positive part.
96h	<b>G_RATIO</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	G_RATIO[7:0]	7:0	Ratio in G channel positive part.
97h	<b>B_BIAS</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	B_BIAS[7:0]	7:0	DC level in B channel positive part.
98h	<b>B_RATIO</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	B_RATIO[7:0]	7:0	Ratio in B channel positive part.
99h	<b>R_BIASN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	R_BIASN[7:0]	7:0	Dc level in R channel negative part.
9Ah	<b>R_RATIO</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	R_RATIO[7:0]	7:0	Ratio in R channel negative part.
9Bh	<b>G_BIASN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	G_BIASN[7:0]	7:0	DC level in G channel negative part.



### Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description
9Ch	<b>G_RATIO</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	G_RATIO[7:0]	7:0	Ratio in G channel negative part.
9Dh	<b>B_BIASN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	B_BIASN[7:0]	7:0	DC level in B channel negative part.
9Eh	<b>B_RATIO</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	B_RATIO[7:0]	7:0	Ratio in B channel negative part.
9Fh	-	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:0	Reserved.

### OSD Register (Bank = 00, Registers A0h ~ AAh)

OSD Register (Bank=00)			
Index	Mnemonic	Bits	Description
A0h	<b>OSDIOA</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	TOSB_MD	7	OSD SRAM I/O Access Burst Mode. 0: Disable. 1: Enable.
	CLR	6	OSD Clear Bit (write only). 0: Normal. 1: Clear code with 00h, attribute with 00h.
	-	5	Reserved.
	RF	4	OSD RAM Font I/O Access. 0: Disable. 1: Enable.
	DC	3	OSD Display Code I/O Access. 0: Disable. 1: Enable.
	DA	2	OSD Display Attribute I/O Access. 0: Disable. 1: Enable.
	ORBW_MD	1	OSD Register Burst Write Mode. 0: Disable. 1: Enable.
	ORBR_MD	0	OSD Register Burst Read Mode. 0: Disable. 1: Enable.

### OSD Register (Bank=00)

Index	Mnemonic	Bits	Description
A1h	<b>OSDRA</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	OSDRA	5:0	OSD Register Address Port.
A2h	<b>OSDRD</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	OSDRD	7:0	OSD Register Data Port.
A3h	<b>OSDFA</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : WO</b>
	OSDFA	7:0	OSD RAM Font Address Port.
A4h	<b>OSDFD</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : WO</b>
	OSDFD	7:0	OSD RAM Font Data Port.
A5h	<b>DISPCA_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : WO</b>
	DISPCA[7:0]	7:0	OSD Display Code Address Port.
A6h	<b>DISPCA_H</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : WO</b>
	-	7:3	Reserved.
	DISPCA[10:8]	2:0	OSD Display Code Address Port.
A7h	<b>DISPCD</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	DISPCD[7:0]	7:0	OSD Display Code Data Port (When write access disabled, this port report display code data).
A8h	<b>DISPAA_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : WO</b>
	DISPAA[7:0]	7:0	OSD Display Attribute Address port.
A9h	<b>DISPAA_H</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : WO</b>
	-	7:3	Reserved.
	DISPAA[10:8]	2:0	OSD Display Attribute Address port.
AAh	<b>DISPAD</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	DISPAD[7:0]	7:0	OSD Display Attribute Data Port (When write access disabled, this port report display attribute data).
AEh	<b>DISPCA_CTL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	DISPAD_RE[8]	6	When write access disabled, this bit report display attribute data (bit 8).
	-	5	Reserved.
	DISPCD_RE[8]	4	When write access disabled, this bit report display code data (bit 8).
-	3	Reserved.	

### OSD Register (Bank=00)

Index	Mnemonic	Bits	Description
	INS_DATA	2	OSD Code/Attribute 9th bit Data (Code (A7h)/Attribute (AAh) Data Extend bit).
	-	1	Reserved.
	CA_NO_WRITE	0	OSD Display Code and Attribute Write disable.
<b>OSD CODE (9th bit)</b>			
	ITALIC	8	OSD Italic Control 0: Disable. 1: Enable. (Please refer AEh bit 0 INS_DATA)
<b>OSD Attribute (8-Color Palette)</b>			
	HALF_TRAN	8	OSD Half-transparency Control. 0: Disable. 1: Enable. (Please refer AEh[0]: INS_DATA and 42h[2]: ALF_TRANEN)
	BLNK_CTRL	7	OSD Blink Control. 0: Disable. 1: Enable.
	FGCLR[2:0]	6:4	OSD Foreground Color Select. 000: Color index 0. 001: Color index 1. ... 111: Color index 7.
	BDER_CTRL	3	OSD Character Border Control. 0: Disable. 1: Enable. (Please refer 42h[5] UNDERLINE_MD)
	BGCLR[2:0]	2:0	OSD Background Color select. 000: color index 0. 001: color index 1. ... 111: color index 7.
<b>OSD Attribute ( 16 Color Palette)</b>			
	FGCLR[3:0]	7:4	OSD Foreground Color Select. 0000: color index 0. 0001: color index 1. ... 1111: color index 15.

### OSD Register (Bank=00)

Index	Mnemonic	Bits	Description
	BGCLR[3:0]	3:0	OSD Background Color Select. 0000: color index 0. 0001: color index 1. ... 1111: color index 15.

### OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)			
Index	Mnemonic	Bits	Description
<b>01h</b>	<b>OSDDBC</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	DBL[1:0]	2:1	Double Buffer Load. 00: Keep old register value. 01: Load new data (auto reset to 00 when loading completes). 10: Automatically load data at VSYNC blanking. 11: Reserved.
	DB_EN	0	Double Buffer Enable. 0: Disable. 1: Enable.
<b>02h</b>	<b>OHSTA-L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	OHSTA[7:0]	7:0	OSD windows Horizontal Start position (pixel) (lower 8 bits).
<b>03h</b>	<b>OHSTA-H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	OHSTA[10:8]	2:0	OSD windows Horizontal Start position (higher 3 bits).
<b>04h</b>	<b>OVSTA-L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	OVSTA[7:0]	7:0	OSD windows Vertical Start position (line) (lower 8 bits).
<b>05h</b>	<b>OVSTA-H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:2	Reserved.
	OVSTA[9:8]	1:0	OSD windows Vertical Start position (higher 2 bits).
<b>06h</b>	<b>OSDW</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	OSDW[5:0]	5:0	OSD windows Width (OSDW + 1 (column)), maximum 64 columns.
<b>07h</b>	<b>OSDH</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.

### OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description
	OSDH[5:0]	5:0	OSD windows Height (OSDH + 1 (row)), maximum 64 rows.
08h	<b>OHSPA</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	OHSPA[5:0]	5:0	OSD windows Horizontal Space start position (OHSPA + 1 (column)).
09h	<b>OVSPA</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	OVSPA[4:0]	4:0	OSD windows Vertical Space start position (OVSPA + 1 (row)).
0Ah	<b>OSPW</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	OSPW[7:0]	7:0	OSD Space Width (8 * OSPW (pixel)).
0Bh	<b>OSPH</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	OSPH[7:0]	7:0	OSD Space Height (8 * OSPH (line)).
0Ch	<b>IOSDC1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	OVS[1:0]	7:6	OSD Vertical Scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.
	OHS[1:0]	5:4	OSD Horizontal Scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.
	-	3:1	Reserved.
	MWIN	0	OSD Main Window display. 0: Off. 1: On.
0Dh	<b>IOSDC2</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	BDC	5	OSD Character Border type select. 0: All direction font boundary (border). 1: Bottom-right direction font boundary (shadow).
	BDW	4	OSD character Border Width control. 0: One pixel with for all scale. 1: Scale with OVS[1:0] and OHS[1:0].
	-	3	Reserved.

**OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)**

Index	Mnemonic	Bits	Description
	BCLR[2:0]	2:0	OSD Border Color index. 000: color index 0. 001: color index 1. ... 111: color index 7.
<b>0Eh</b>	<b>IOSDC3</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	-	7:6	Reserved.
	SHALL	5	OSD Shadow with All Direction. 0: Shadow with Bottom-Right direction (shadow). 1: Shadow with all direction (border).
	SDC	4	OSD Window Shadow Control. 0: Off. 1: On.
	SCLR[3:0]	3:0	OSD window Shadow Color index. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index 15.
<b>0Fh</b>	<b>OSHC</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	OSDSH[3:0]	7:4	OSD Shadow Height.
	OSDSW[3:0]	3:0	OSD Shadow Width.
<b>10h</b>	<b>IOSDC4</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	LINE_SHIFT_EN	7	OSD line shift Enable (Please refer 45h bit 4~2 LINE_SHIFT_VAL).
	FIELD_POL	6	OSD line shift Field Polarity.
	-	5	Reserved.
	EN_M4C	4	4 Color Font Enable. 0: Disable. 1: Enable.
	F16H	3	OSD font high control. 0: Font height is 18. 1: Font height is 16.
	PEXT	2	OSD 16 color palette extent method. 0: Extend with palette bit 3. 1: Extend with 0.

**OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)**

Index	Mnemonic	Bits	Description
	TRANEN	1	OSD Transparency Enable. 0: No transparency. 1: Color index which hit OSD Color index for transparency[2:0] is transparent of 8 color palette/ Color index which hit OSD Color index for transparency[3:0] is transparent of 16 color palette. (Please refer 42h bit 3~0 OSD Color index for transparency.)
	T16C	0	OSD 16 Color Palette select. 0: 8 color palette. 1: 16 color palette.
<b>12h</b>	<b>OCBUFO</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CO_SEL	7	OSD Code buffer Offset Select. 0: Use OSDW[5:0] as offset. 1: Use OOFFSET[5:0] as offset.
	-	6	Reserved.
	OOFFSET[5:0]	5:0	OSD code buffer Offset Value.
<b>13h</b>	<b>OSDBA-L</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	OSDBA[7:0]	7:0	OSD code Base Address (lower 8 bits).
<b>14h</b>	<b>OSDBA-H</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	-	7:3	Reserved.
	OSDBA[10:8]	2:0	OSD code Base Address (higher 3 bits) (Please refer 45h bit7 CCRAM608X2. When CCRAM608X2 = 0, OSDBA[10:0] is programming from 0 to 4BFh; when CCRAM608X2 = 1, OSDBA[9:0] is programming from 0 to 25fh and OSDBA[10] is programming to select low or high part code/attribute SRAM).
<b>15h</b>	<b>GCCTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	GVS[1:0]	7:6	Gradually color Vertical Scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.
	GHS[1:0]	5:4	Gradually color Horizontal Scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.

**OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)**

Index	Mnemonic	Bits	Description
	GRAD	3	Enable OSD Gradual color function. 0: Disable. 1: Enable.
	ADC_PG	2	ADC Pattern Generator select. 0: Normal. 1: ADC.
	-	1:0	Reserved.
<b>16h</b>	<b>GRADCLR</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	FCLR	7	Gradual color by Frame Color. 0: Use RCLR, GCLR, BCLR as starting gradual color. 1: Use Frame Color as starting gradual color.
	-	6	Reserved.
	RCLR[1:0]	5:4	Red starting gradual Color. 00: Red color is 00h. 01: Red color is 55h. 10: Red color is AAh. 11: Red color is FFh.
	GCLR[1:0]	3:2	Green starting gradual Color. 00: Green color is 00h. 01: Green color is 55h. 10: Green color is AAh. 11: Green color is FFh.
	BCLR[1:0]	1:0	Blue starting gradual Color. 00: Blue color is 00h. 01: Blue color is 55h. 10: Blue color is AAh. 11: Blue color is FFh.
<b>17h</b>	<b>HGRADCR</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SR	7	Sign bit of Red color. 0: Increase. 1: Decrease.
	IRH	6	Inverse bit of Red color. 0: Normal. 1: Invert.
	R_GRADH[5:0]	5:0	Increase/decrease value of Red color.
<b>18h</b>	<b>HGRADCG</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>



### OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description
	SG	7	Sign bit of Green color. 0: Increase. 1: Decrease.
	IGH	6	Inverse bit of Green color. 0: Normal. 1: Invert.
	G_GRADH[5:0]	5:0	Increase/decrease value of Green color.
<b>19h</b>	<b>HGRADCB</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SB	7	Sign bit of Blue color. 0: Increase. 1: Decrease.
	IBH	6	Inverse bit of Blue color. 0: Normal. 1: Invert.
	B_GRADH[5:0]	5:0	Increase/decrease value of Blue color.
<b>1Ah</b>	<b>HGRADSR</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	HGRADSR[7:0]	7:0	Horizontal Gradual Step of Red color.
<b>1Bh</b>	<b>HGRADSG</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	HGRADSG[7:0]	7:0	Horizontal Gradual Step of Green color.
<b>1Ch</b>	<b>HGRADSB</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	HGRADSB[7:0]	7:0	Horizontal Gradual Step of Blue color.
<b>1Dh</b>	<b>VGRADCR</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SR	7	Sign bit of Red color. 0: Increase. 1: Decrease.
	IRV	6	Inverse bit of Red color. 0: Normal. 1: Invert.
	R_GRADV[5:0]	5:0	Increase/decrease value of Red color.
<b>1Eh</b>	<b>VGRADCG</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SG	7	Sign bit of Green color. 0: Increase. 1: Decrease.
	IGV	6	Inverse bit of Green color. 0: Normal. 1: Invert.

### OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description
	G_GRADV[5:0]	5:0	Increase/Decrease value of Green color.
1Fh	<b>VGRADCB</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SB	7	Sign bit of Blue color. 0: Increase. 1: Decrease.
	IBV	6	Inverse bit of Blue color. 0: Normal. 1: Invert.
	B_GRADV[5:0]	5:0	Increase/decrease value of Blue color.
20h	<b>VGRADSR</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	VGRADSR[7:0]	7:0	Vertical Gradual Step of Red color.
21h	<b>VGRADSG</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	VGRADSG[7:0]	7:0	Vertical Gradual Step of Green color.
22h	<b>VGRADSB</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	VGRADSB[7:0]	7:0	Vertical Gradual Step of Blue color.
23h ~	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
25h	-	7:0	Reserved.
26h	<b>TIMECTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	FRG_EN	4	OSD Font Ram Gated Enable. 0: Disable. 1: Enable.
	-	3:2	Reserved
	VSTDLY	1	OSD Vertical Start Delay. 0: Normal. 1: Vertical Delay 1 line.
	-	0	Reserved.
27h	<b>OSDRTP</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	RTPT	2	OSD Random Test Pattern Type. 0: RGB is the same. 1: RGB is different.

### OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description
	OSDRTP[1:0]	1:0	OSD Random Test Pattern. 00: Disable. 01: 1 random bit. 10: 2 random bit. 11: Reserved.
<b>OSD Color Palette when T16_C = 0</b>			
<b>28h</b>	<b>CLR0R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR0R[7:0]	7:0	Red Color Index 0.
<b>29h</b>	<b>CLR0G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR0G[7:0]	7:0	Green Color Index 0.
<b>2Ah</b>	<b>CLR0B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR0B[7:0]	7:0	Blue Color Index 0.
<b>2Bh</b>	<b>CLR1R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR1R[7:0]	7:0	Red Color Index 1.
<b>2Ch</b>	<b>CLR1G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR1G[7:0]	7:0	Green Color Index 1.
<b>2Dh</b>	<b>CLR1B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR1B[7:0]	7:0	Blue Color Index 1.
<b>2Eh</b>	<b>CLR2R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR2R[7:0]	7:0	Red Color Index 2.
<b>2Fh</b>	<b>CLR2G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR2G[7:0]	7:0	Green Color Index 2.
<b>30h</b>	<b>CLR2B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR2B[7:0]	7:0	Blue Color Index 2.
<b>31h</b>	<b>CLR3R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR3R[7:0]	7:0	Red Color Index 3.
<b>32h</b>	<b>CLR3G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR3G[7:0]	7:0	Green Color Index 3.
<b>33h</b>	<b>CLR3B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR3B[7:0]	7:0	Blue Color Index 3.
<b>34h</b>	<b>CLR4R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR4R[7:0]	7:0	Red Color Index 4.
<b>35h</b>	<b>CLR4G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>

**OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)**

Index	Mnemonic	Bits	Description
	CLR4G[7:0]	7:0	Green Color Index 4.
36h	<b>CLR4B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR4B[7:0]	7:0	Blue Color Index 4.
37h	<b>CLR5R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR5R[7:0]	7:0	Red Color Index 5.
38h	<b>CLR5G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR5G[7:0]	7:0	Green Color Index 5.
39h	<b>CLR5B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR5B[7:0]	7:0	Blue Color Index 5.
3Ah	<b>CLR6R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR6R[7:0]	7:0	Red Color Index 6.
3Bh	<b>CLR6G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR6G[7:0]	7:0	Green Color Index 6.
3Ch	<b>CLR6B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR6B[7:0]	7:0	Blue Color Index 6.
3Dh	<b>CLR7R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR7R[7:0]	7:0	Red Color Index 7.
3Eh	<b>CLR7G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR7G[7:0]	7:0	Green Color Index 7.
3Fh	<b>CLR7B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR7B[7:0]	7:0	Blue Color Index 7.
<b>OSD Color Palette when T16_C = 1 (16 color format: col[7:4], 4'b0 or col[7:4], {4{col[4]}})</b>			
28h	<b>CLR0R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR0R[7:4]	7:4	Red Color Index 0.
	CLR8R[3:0]	3:0	Red Color Index 8.
29h	<b>CLR0G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR0G[7:4]	7:4	Green Color Index 0.
	CLR8G[3:0]	3:0	Green Color Index 8.
2Ah	<b>CLR0B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLR0B[7:4]	7:4	Blue Color Index 0.
	CLR8B[3:0]	3:0	Blue Color Index 8.
2Bh	<b>CLR1R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>

**OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)**

Index	Mnemonic	Bits	Description
	CLR1R[7:4]	7:4	Red Color Index 1.
	CLR9R[3:0]	3:0	Red Color Index 9.
<b>2Ch</b>	<b>CLR1G</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR1G[7:4]	7:4	Green Color Index 1.
	CLR9G[3:0]	3:0	Green Color Index 9.
<b>2Dh</b>	<b>CLR1B</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR1B[7:4]	7:4	Blue Color Index 1.
	CLR9B[3:0]	3:0	Blue Color Index 9.
<b>2Eh</b>	<b>CLR2R</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR2R[7:4]	7:4	Red Color Index 2.
	CLR10R[3:0]	3:0	Red Color Index 10.
<b>2Fh</b>	<b>CLR2G</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR2G[7:4]	7:4	Green Color Index 2.
	CLR10G[3:0]	3:0	Green Color Index 10.
<b>30h</b>	<b>CLR2B</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR2B[7:4]	7:4	Blue Color Index 2.
	CLR10B[3:0]	3:0	Blue Color Index 10.
<b>31h</b>	<b>CLR3R</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR3R[7:4]	7:4	Red Color Index 3.
	CLR11R[3:0]	3:0	Red Color Index 11.
<b>32h</b>	<b>CLR3G</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR3G[7:4]	7:4	Green Color Index 3.
	CLR11G[3:0]	3:0	Green Color Index 11.
<b>33h</b>	<b>CLR3B</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR3B[7:4]	7:4	Blue Color Index 3.
	CLR11B[3:0]	3:0	Blue Color Index 11.
<b>34h</b>	<b>CLR4R</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR4R[7:4]	7:4	Red Color Index 4.
	CLR12R[3:0]	3:0	Red Color Index 12.
<b>35h</b>	<b>CLR4G</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR4G[7:4]	7:4	Green Color Index 4.
	CLR12G[3:0]	3:0	Green Color Index 12.

**OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)**

Index	Mnemonic	Bits	Description
<b>36h</b>	<b>CLR4B</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR4B[7:4]	7:4	Blue Color Index 4.
	CLR12B[3:0]	3:0	Blue Color Index 12.
<b>37h</b>	<b>CLR5R</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR5R[7:4]	7:4	Red Color Index 5.
	CLR13R[3:0]	3:0	Red Color Index 13.
<b>38h</b>	<b>CLR5G</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR5G[7:4]	7:4	Green Color Index 5.
	CLR13G[3:0]	3:0	Green Color Index 13.
<b>39h</b>	<b>CLR5B</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR5B[7:4]	7:4	Blue Color Index 5.
	CLR13B[3:0]	3:0	Blue Color Index 13.
<b>3Ah</b>	<b>CLR6R</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR6R[7:4]	7:4	Red Color Index 6.
	CLR14R[3:0]	3:0	Red Color Index 14.
<b>3Bh</b>	<b>CLR6G</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR6G[7:4]	7:4	Green Color Index 6.
	CLR14G[3:0]	3:0	Green Color Index 14.
<b>3Ch</b>	<b>CLR6B</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR6B[7:4]	7:4	Blue Color Index 6.
	CLR14B[3:0]	3:0	Blue Color Index 14.
<b>3Dh</b>	<b>CLR7R</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR7R[7:4]	7:4	Red Color Index 7.
	CLR15R[3:0]	3:0	Red Color Index 15.
<b>3Eh</b>	<b>CLR7G</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR7G[7:4]	7:4	Green Color Index 7.
	CLR15G[3:0]	3:0	Green Color Index 15.
<b>3Fh</b>	<b>CLR7B</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLR7B[7:4]	7:4	Blue Color Index 7.
	CLR15B[3:0]	3:0	Blue Color Index 15.
<b>40h</b>	<b>SCRLSPD</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	SCRLSPD[7:0]	7:0	OSD Scroll function speed (the numbers of VSYNC).

### OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description
<b>41h</b>	<b>SCROLLINE</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SCREN	7	OSD Scroll function Enable. 0: Disable. 1: Enable.
	VSCR_FAST	6	Scroll at every VSYNC.
	TRUC_EN	5	Truncate code/attribute Enable. 0: Disable. 1: Enable.
	SCROLLINE[4:0]	4:0	OSD Scroll function (the numbers of scan lines per scroll).
<b>42h</b>	<b>UNDERLINE</b>	<b>7:0</b>	<b>Default : 0x0F</b> <b>Access : R/W</b>
	UNDERLINE_1	7	OSD Underline at last line.
	UNDERLINE_2	6	OSD Underline at second last line.
	UNDERLINE_MD	5	OSD Underline Mode enable (When this bit is asserted, OSD Attribute (8 Color) bit 3. (BDER) Character Boder Control change function to OSD Character Underline Control).
	HALF_TRANEN	4	OSD Half-Transparency Enable (When this bit is asserted, OSD Attribute (8 Color) bit 9 (HALF_TRAN) is active.).
	TRAN_INDEX[3:0]	3:0	OSD Color Index for Transparency (Define which color index is transparent).
<b>43h</b>	<b>TRUNCATE</b>	<b>7:0</b>	<b>Default : 0x 1D</b> <b>Access : R/W</b>
	TRUNCATENUM	7:0	OSD Truncate number (Please refer 45h bit7 CCRAM608X2. When CCRAM608X2=0, final row=(11'h4bf-TRUNCATENUM); when CCRAM608X2=1, final row=(11'h25f-TRUNCATENUM)).
<b>44h</b>	<b>ITALIC</b>	<b>7:0</b>	<b>Default : 0x 00</b> <b>Access : R/W</b>
	ITALIC_OFFSET	7:6	OSD Italic right shift Offset (00: 1, 01: 2, 10: 3, 11: 4 (pixel)).
	ITALIC_1ST_LINE	5:4	OSD Italic start scan Line (00: 0, 01: 1, 10: 2, 11: 3 (line)).
	ITALIC_STEP	3:2	OSD Italic left shift Step (00: 0.001, 01: 0.010, 10: 0.011, 11: 0.100 (pixel , binary)).
	ITALIC_EN	1	OSD Italic function Enable. 0: Disable. 1: Enable.
	-	0	Reserved.
<b>45h</b>	<b>MISC_CTL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CCRAM608X2	7	OSD 2 608 code/attribute SRAM (When CCRAM608X2 = 0, there is one 1216 code/attribute SRAM for using; when CCRAM608X2 = 1, there are two 608 code/attribute SRAM for using.).

### OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description
	-	6:5	Reserved.
	LINE_SHIFT_VAL[2:0]	4:2	OSD Line shift value (Line shift number, 000: 1, ..., 111: 8).
	CARHG_EN	1	OSD code/attribute high part ram gated Enable. 0: Disable. 1: Enable.
	-	0	Reserved.
<b>46h</b>	<b>OSD4CFFA</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	OSD4CFFA[7:0]	7:0	OSD 4 Color Font RAM start Address (must be even number).
<b>47h ~ 49h</b>	-	<b>7:0</b>	<b>Default : -</b> <span style="float: right;"><b>Access : -</b></span>
	-	7:0	Reserved.
<b>4Ah</b>	<b>OHVSTA-H</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : RO</b></span>
	VSCR_OPT	7	Vscroll Option. 0: Original. 1: Fixed.
	-	6	Reserved.
	OVSTA[9:8]	5:4	OSD windows Vertical Start position (Read only).
	-	3	Reserved.
	OHSTA[10:8]	2:0	OSD windows Horizontal Start position. (Read only).
<b>4Bh ~ 4Ch</b>	-	<b>7:0</b>	<b>Default : -</b> <span style="float: right;"><b>Access : -</b></span>
	-	7:0	Reserved.
<b>4Dh</b>	<b>OSDBRI</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	OSDBRI_EN	7	OSD Brightness Enable. 0: Disable. 1: Enable.
	OSDBRI_DIR	6	OSD Brightness Control. 0: Add. 1: Subtract.
	OSDBRI_VAL[5:0]	5:0	OSD Brightness Value.
<b>4Eh ~ 4Fh</b>	-	<b>7:0</b>	<b>Default : -</b> <span style="float: right;"><b>Access : -</b></span>
	-	7:0	Reserved.
<b>50h</b>	<b>CODECLRDATA_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	CODECLRDATA[7:0]	7:0	OSD Code Clear Data.
<b>51h</b>	<b>ATRCLRDATA_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	ATRCLRDATA[7:0]	7:0	OSD Attribute Clear Data (lower 8 bits).



**OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)**

Index	Mnemonic	Bits	Description
52h	<b>OSDCLRDATA</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	ATRCLRDATA[8]	4	OSD Attribute Clear Data.
	-	3:1	Reserved.
	CODECLRDATA[8]	0	OSD Code Clear Data.
53h	<b>OSDCLRADR_L</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	OSDCLR_ADR[7:0]	7:0	OSD Clear Starting address (lower 8 bits).
54h	<b>OSDCLRADR_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	ATR1_CLREN	7	OSD Attribute High Clear Enable.
	ATR0_CLREN	6	OSD Attribute Low Clear Enable.
	CODE1_CLREN	5	OSD Code High Clear Enable.
	CODE0_CLREN	4	OSD Code Low Clear Enable.
	-	3:2	Reserved.
	OSDCLR_ADR[9:8]	1:0	OSD Clear Starting Address.
55h	<b>OSDCLR_OFST</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	OSDCLR_OFST[6:0]	6:0	OSD Clear Offset.
56h	<b>OSDCLR_WID</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	OSDCLR_WID[6:0]	6:0	OSD Clear Width.
57h	<b>OSDCLR_HIGT</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	OSDCLR_HIGT[6:0]	6:0	OSD Clear Height.
58h	<b>OSDCLR_CTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:1	Reserved.
	BLK_CLR_EN	0	OSD Block Clear Enable.
59h ~ 9Fh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.

## Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)

Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)				
Index	Mnemonic	Bits	Description	
00h	<b>Gamma_R00</b>	<b>7:0</b>	<b>Default : 0d00</b>	<b>Access : R/W</b>
	Gamma_R00	7:0	Gamma_table R00 value.	
01h	<b>Gamma_R01</b>	<b>7:0</b>	<b>Default : 0d07</b>	<b>Access : R/W</b>
	Gamma_R01	7:0	Gamma_table R01 value.	
02h	<b>Gamma_R02</b>	<b>7:0</b>	<b>Default : 0d15</b>	<b>Access : R/W</b>
	Gamma_R02	7:0	Gamma_table R02 value.	
03h	<b>Gamma_R03</b>	<b>7:0</b>	<b>Default : 0d23</b>	<b>Access : R/W</b>
	Gamma_R03	7:0	Gamma_table R03 value.	
04h	<b>Gamma_R04</b>	<b>7:0</b>	<b>Default : 0d31</b>	<b>Access : R/W</b>
	Gamma_R04	7:0	Gamma_table R04 value.	
05h	<b>Gamma_R05</b>	<b>7:0</b>	<b>Default : 0d39</b>	<b>Access : R/W</b>
	Gamma_R05	7:0	Gamma_table R05 value.	
06h	<b>Gamma_R06</b>	<b>7:0</b>	<b>Default : 0d47</b>	<b>Access : R/W</b>
	Gamma_R06	7:0	Gamma_table R06 value.	
07h	<b>Gamma_R07</b>	<b>7:0</b>	<b>Default : 0d55</b>	<b>Access : R/W</b>
	Gamma_R07	7:0	Gamma_table R07 value.	
08h	<b>Gamma_R08</b>	<b>7:0</b>	<b>Default : 0d63</b>	<b>Access : R/W</b>
	Gamma_R08	7:0	Gamma_table R08 value.	
09h	<b>Gamma_R09</b>	<b>7:0</b>	<b>Default : 0d71</b>	<b>Access : R/W</b>
	Gamma_R09	7:0	Gamma_table R09 value.	
0Ah	<b>Gamma_R10</b>	<b>7:0</b>	<b>Default : 0d79</b>	<b>Access : R/W</b>
	Gamma_R10	7:0	Gamma_table R10 value.	
0Bh	<b>Gamma_R11</b>	<b>7:0</b>	<b>Default : 0d87</b>	<b>Access : R/W</b>
	Gamma_R11	7:0	Gamma_table R11 value.	
0Ch	<b>Gamma_R12</b>	<b>7:0</b>	<b>Default : 0d95</b>	<b>Access : R/W</b>
	Gamma_R12	7:0	Gamma_table R12 value.	
0Dh	<b>Gamma_R13</b>	<b>7:0</b>	<b>Default : 0d103</b>	<b>Access : R/W</b>
	Gamma_R13	7:0	Gamma_table R13 value.	
0Eh	<b>Gamma_R14</b>	<b>7:0</b>	<b>Default : 0d111</b>	<b>Access : R/W</b>
	Gamma_R14	7:0	Gamma_table R14 value.	
0Fh	<b>Gamma_R15</b>	<b>7:0</b>	<b>Default : 0d119</b>	<b>Access : R/W</b>
	Gamma_R15	7:0	Gamma_table R15 value.	

### Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)

Index	Mnemonic	Bits	Description
10h	<b>Gamma_R16</b>	<b>7:0</b>	<b>Default : 0d127</b> <b>Access : R/W</b>
	Gamma_R16	7:0	Gamma_table R16 value.
11h	<b>Gamma_R17</b>	<b>7:0</b>	<b>Default : 0d135</b> <b>Access : R/W</b>
	Gamma_R17	7:0	Gamma_table R17 value.
12h	<b>Gamma_R18</b>	<b>7:0</b>	<b>Default : 0d143</b> <b>Access : R/W</b>
	Gamma_R18	7:0	Gamma_table R18 value.
13h	<b>Gamma_R19</b>	<b>7:0</b>	<b>Default : 0d151</b> <b>Access : R/W</b>
	Gamma_R49	7:0	Gamma_table R19 value.
14h	<b>Gamma_R20</b>	<b>7:0</b>	<b>Default : 0d159</b> <b>Access : R/W</b>
	Gamma_R20	7:0	Gamma_table R20 value.
15h	<b>Gamma_R21</b>	<b>7:0</b>	<b>Default : 0d167</b> <b>Access : R/W</b>
	Gamma_R21	7:0	Gamma_table R21 value.
16h	<b>Gamma_R22</b>	<b>7:0</b>	<b>Default : 0d175</b> <b>Access : R/W</b>
	Gamma_R22	7:0	Gamma_table R22 value.
17h	<b>Gamma_R23</b>	<b>7:0</b>	<b>Default : 0d183</b> <b>Access : R/W</b>
	Gamma_R23	7:0	Gamma_table R23 value.
18h	<b>Gamma_R24</b>	<b>7:0</b>	<b>Default : 0d191</b> <b>Access : R/W</b>
	Gamma_R24	7:0	Gamma_table R24 value.
19h	<b>Gamma_R25</b>	<b>7:0</b>	<b>Default : 0d199</b> <b>Access : R/W</b>
	Gamma_R25	7:0	Gamma_table R25 value.
1Ah	<b>Gamma_R26</b>	<b>7:0</b>	<b>Default : 0d207</b> <b>Access : R/W</b>
	Gamma_R26	7:0	Gamma_table R26 value.
1Bh	<b>Gamma_R27</b>	<b>7:0</b>	<b>Default : 0d215</b> <b>Access : R/W</b>
	Gamma_R27	7:0	Gamma_table R27 value.
1Ch	<b>Gamma_R28</b>	<b>7:0</b>	<b>Default : 0d223</b> <b>Access : R/W</b>
	Gamma_R28	7:0	Gamma_table R28 value.
1Dh	<b>Gamma_R29</b>	<b>7:0</b>	<b>Default : 0d232</b> <b>Access : R/W</b>
	Gamma_R29	7:0	Gamma_table R29 value.
1Eh	<b>Gamma_R30</b>	<b>7:0</b>	<b>Default : 0d239</b> <b>Access : R/W</b>
	Gamma_R30	7:0	Gamma_table R30 value.
1Fh	<b>Gamma_R31</b>	<b>7:0</b>	<b>Default : 0d247</b> <b>Access : R/W</b>
	Gamma_R31	7:0	Gamma_table R31 value.
20h	<b>Gamma_R32</b>	<b>7:0</b>	<b>Default : 0d255</b> <b>Access : R/W</b>

### Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)

Index	Mnemonic	Bits	Description
	Gamma_R32	7:0	Gamma_table R32 value.
21h	<b>Gamma_G00</b>	<b>7:0</b>	<b>Default : 0d00</b> <b>Access : R/W</b>
	Gamma_G00	7:0	Gamma_table G00 value.
22h	<b>Gamma_G01</b>	<b>7:0</b>	<b>Default : 0d07</b> <b>Access : R/W</b>
	Gamma_G01	7:0	Gamma_table G01 value.
23h	<b>Gamma_G02</b>	<b>7:0</b>	<b>Default : 0d15</b> <b>Access : R/W</b>
	Gamma_G02	7:0	Gamma_table G02 value.
24h	<b>Gamma_G03</b>	<b>7:0</b>	<b>Default : 0d23</b> <b>Access : R/W</b>
	Gamma_G03	7:0	Gamma_table G03 value.
25h	<b>Gamma_G04</b>	<b>7:0</b>	<b>Default : 0d31</b> <b>Access : R/W</b>
	Gamma_G04	7:0	Gamma_table G04 value.
26h	<b>Gamma_G05</b>	<b>7:0</b>	<b>Default : 0d39</b> <b>Access : R/W</b>
	Gamma_G05	7:0	Gamma_table G05 value.
27h	<b>Gamma_G06</b>	<b>7:0</b>	<b>Default : 0d47</b> <b>Access : R/W</b>
	Gamma_G06	7:0	Gamma_table G06 value.
28h	<b>Gamma_G07</b>	<b>7:0</b>	<b>Default : 0d55</b> <b>Access : R/W</b>
	Gamma_G07	7:0	Gamma_table G07 value.
29h	<b>Gamma_G08</b>	<b>7:0</b>	<b>Default : 0d63</b> <b>Access : R/W</b>
	Gamma_G08	7:0	Gamma_table G08 value.
2Ah	<b>Gamma_G09</b>	<b>7:0</b>	<b>Default : 0d71</b> <b>Access : R/W</b>
	Gamma_G09	7:0	Gamma_table G09 value.
2Bh	<b>Gamma_G10</b>	<b>7:0</b>	<b>Default : 0d79</b> <b>Access : R/W</b>
	Gamma_G10	7:0	Gamma_table G10 value.
2Ch	<b>Gamma_G11</b>	<b>7:0</b>	<b>Default : 0d87</b> <b>Access : R/W</b>
	Gamma_G11	7:0	Gamma_table G11 value.
2Dh	<b>Gamma_G12</b>	<b>7:0</b>	<b>Default : 0d95</b> <b>Access : R/W</b>
	Gamma_G12	7:0	Gamma_table G12 value.
2Eh	<b>Gamma_G13</b>	<b>7:0</b>	<b>Default : 0d103</b> <b>Access : R/W</b>
	Gamma_G13	7:0	Gamma_table G13 value.
2Fh	<b>Gamma_G14</b>	<b>7:0</b>	<b>Default : 0d111</b> <b>Access : R/W</b>
	Gamma_G14	7:0	Gamma_table G14 value.
30h	<b>Gamma_G15</b>	<b>7:0</b>	<b>Default : 0d119</b> <b>Access : R/W</b>
	Gamma_G15	7:0	Gamma_table G15 value.

**Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)**

Index	Mnemonic	Bits	Description
31h	<b>Gamma_G16</b>	<b>7:0</b>	<b>Default : 0d127</b> <b>Access : R/W</b>
	Gamma_G16	7:0	Gamma_table G16 value.
32h	<b>Gamma_G17</b>	<b>7:0</b>	<b>Default : 0d135</b> <b>Access : R/W</b>
	Gamma_G17	7:0	Gamma_table G17 value.
33h	<b>Gamma_G18</b>	<b>7:0</b>	<b>Default : 0d143</b> <b>Access : R/W</b>
	Gamma_G18	7:0	Gamma_table G18 value.
34h	<b>Gamma_G19</b>	<b>7:0</b>	<b>Default : 0d151</b> <b>Access : R/W</b>
	Gamma_G19	7:0	Gamma_table G19 value.
35h	<b>Gamma_G20</b>	<b>7:0</b>	<b>Default : 0d159</b> <b>Access : R/W</b>
	Gamma_G20	7:0	Gamma_table G20 value.
36h	<b>Gamma_G21</b>	<b>7:0</b>	<b>Default : 0d167</b> <b>Access : R/W</b>
	Gamma_G21	7:0	Gamma_table G21 value.
37h	<b>Gamma_G22</b>	<b>7:0</b>	<b>Default : 0d175</b> <b>Access : R/W</b>
	Gamma_G22	7:0	Gamma_table G22 value.
38h	<b>Gamma_G23</b>	<b>7:0</b>	<b>Default : 0d183</b> <b>Access : R/W</b>
	Gamma_G23	7:0	Gamma_table G23 value.
39h	<b>Gamma_G24</b>	<b>7:0</b>	<b>Default : 0d191</b> <b>Access : R/W</b>
	Gamma_G24	7:0	Gamma_table G24 value.
3Ah	<b>Gamma_G25</b>	<b>7:0</b>	<b>Default : 0d199</b> <b>Access : R/W</b>
	Gamma_G25	7:0	Gamma_table G25 value.
3Bh	<b>Gamma_G26</b>	<b>7:0</b>	<b>Default : 0d207</b> <b>Access : R/W</b>
	Gamma_G26	7:0	Gamma_table G26 value.
3Ch	<b>Gamma_G27</b>	<b>7:0</b>	<b>Default : 0d215</b> <b>Access : R/W</b>
	Gamma_G27	7:0	Gamma_table G27 value.
3Dh	<b>Gamma_G28</b>	<b>7:0</b>	<b>Default : 0d223</b> <b>Access : R/W</b>
	Gamma_G28	7:0	Gamma_table G28 value.
3Eh	<b>Gamma_G29</b>	<b>7:0</b>	<b>Default : 0d232</b> <b>Access : R/W</b>
	Gamma_G29	7:0	Gamma_table G29 value.
3Fh	<b>Gamma_G30</b>	<b>7:0</b>	<b>Default : 0d239</b> <b>Access : R/W</b>
	Gamma_G30	7:0	Gamma_table G30 value.
40h	<b>Gamma_G31</b>	<b>7:0</b>	<b>Default : 0d247</b> <b>Access : R/W</b>
	Gamma_G31	7:0	Gamma_table G31 value.
41h	<b>Gamma_G32</b>	<b>7:0</b>	<b>Default : 0d255</b> <b>Access : R/W</b>

### Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)

Index	Mnemonic	Bits	Description
	Gamma_G32	7:0	Gamma_table G32 value.
42h	<b>Gamma_B00</b>	<b>7:0</b>	<b>Default : 0d00</b> <b>Access : R/W</b>
	Gamma_B00	7:0	Gamma_table B00 value.
43h	<b>Gamma_B01</b>	<b>7:0</b>	<b>Default : 0d07</b> <b>Access : R/W</b>
	Gamma_B01	7:0	Gamma_table B01 value.
44h	<b>Gamma_B02</b>	<b>7:0</b>	<b>Default : 0d15</b> <b>Access : R/W</b>
	Gamma_B02	7:0	Gamma_table B02 value.
45h	<b>Gamma_B03</b>	<b>7:0</b>	<b>Default : 0d23</b> <b>Access : R/W</b>
	Gamma_B03	7:0	Gamma_table B03 value.
46h	<b>Gamma_B04</b>	<b>7:0</b>	<b>Default : 0d31</b> <b>Access : R/W</b>
	Gamma_B04	7:0	Gamma_table B04 value.
47h	<b>Gamma_B05</b>	<b>7:0</b>	<b>Default : 0d39</b> <b>Access : R/W</b>
	Gamma_B05	7:0	Gamma_table B05 value.
48h	<b>Gamma_B06</b>	<b>7:0</b>	<b>Default : 0d47</b> <b>Access : R/W</b>
	Gamma_B06	7:0	Gamma_table B06 value.
49h	<b>Gamma_B07</b>	<b>7:0</b>	<b>Default : 0d55</b> <b>Access : R/W</b>
	Gamma_B07	7:0	Gamma_table B07 value.
4Ah	<b>Gamma_B08</b>	<b>7:0</b>	<b>Default : 0d63</b> <b>Access : R/W</b>
	Gamma_B08	7:0	Gamma_table B08 value.
4Bh	<b>Gamma_B09</b>	<b>7:0</b>	<b>Default : 0d71</b> <b>Access : R/W</b>
	Gamma_B09	7:0	Gamma_table B09 value.
4Ch	<b>Gamma_B10</b>	<b>7:0</b>	<b>Default : 0d79</b> <b>Access : R/W</b>
	Gamma_B10	7:0	Gamma_table B10 value.
4Dh	<b>Gamma_B11</b>	<b>7:0</b>	<b>Default : 0d87</b> <b>Access : R/W</b>
	Gamma_B11	7:0	Gamma_table B11 value.
4Eh	<b>Gamma_B12</b>	<b>7:0</b>	<b>Default : 0d95</b> <b>Access : R/W</b>
	Gamma_B12	7:0	Gamma_table B12 value.
4Fh	<b>Gamma_B13</b>	<b>7:0</b>	<b>Default : 0d103</b> <b>Access : R/W</b>
	Gamma_B13	7:0	Gamma_table B13 value.
50h	<b>Gamma_B14</b>	<b>7:0</b>	<b>Default : 0d111</b> <b>Access : R/W</b>
	Gamma_B14	7:0	Gamma_table B14 value.
51h	<b>Gamma_B15</b>	<b>7:0</b>	<b>Default : 0d119</b> <b>Access : R/W</b>
	Gamma_B15	7:0	Gamma_table B15 value.

### Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)

Index	Mnemonic	Bits	Description
52h	<b>Gamma_B16</b>	<b>7:0</b>	<b>Default : 0d127</b> <b>Access : R/W</b>
	Gamma_B16	7:0	Gamma_table B16 value.
53h	<b>Gamma_B17</b>	<b>7:0</b>	<b>Default : 0d135</b> <b>Access : R/W</b>
	Gamma_B17	7:0	Gamma_table B17 value.
54h	<b>Gamma_B18</b>	<b>7:0</b>	<b>Default : 0d143</b> <b>Access : R/W</b>
	Gamma_B18	7:0	Gamma_table B18 value.
55h	<b>Gamma_B19</b>	<b>7:0</b>	<b>Default : 0d151</b> <b>Access : R/W</b>
	Gamma_B19	7:0	Gamma_table B19 value.
56h	<b>Gamma_B20</b>	<b>7:0</b>	<b>Default : 0d159</b> <b>Access : R/W</b>
	Gamma_B20	7:0	Gamma_table B20 value.
57h	<b>Gamma_B21</b>	<b>7:0</b>	<b>Default : 0d167</b> <b>Access : R/W</b>
	Gamma_B21	7:0	Gamma_table B21 value.
58h	<b>Gamma_B22</b>	<b>7:0</b>	<b>Default : 0d175</b> <b>Access : R/W</b>
	Gamma_B22	7:0	Gamma_table B22 value.
59h	<b>Gamma_B23</b>	<b>7:0</b>	<b>Default : 0d183</b> <b>Access : R/W</b>
	Gamma_B23	7:0	Gamma_table B23 value.
5Ah	<b>Gamma_B24</b>	<b>7:0</b>	<b>Default : 0d191</b> <b>Access : R/W</b>
	Gamma_B24	7:0	Gamma_table B24 value.
5Bh	<b>Gamma_B25</b>	<b>7:0</b>	<b>Default : 0d199</b> <b>Access : R/W</b>
	Gamma_B25	7:0	Gamma_table B25 value.
5Ch	<b>Gamma_B26</b>	<b>7:0</b>	<b>Default : 0d207</b> <b>Access : R/W</b>
	Gamma_B26	7:0	Gamma_table B26 value.
5Dh	<b>Gamma_B27</b>	<b>7:0</b>	<b>Default : 0d215</b> <b>Access : R/W</b>
	Gamma_B27	7:0	Gamma_table B27 value.
5Eh	<b>Gamma_B28</b>	<b>7:0</b>	<b>Default : 0d223</b> <b>Access : R/W</b>
	Gamma_B28	7:0	Gamma_table B28 value.
5Fh	<b>Gamma_B29</b>	<b>7:0</b>	<b>Default : 0d232</b> <b>Access : R/W</b>
	Gamma_B29	7:0	Gamma_table B29 value.
60h	<b>Gamma_B30</b>	<b>7:0</b>	<b>Default : 0d239</b> <b>Access : R/W</b>
	Gamma_B30	7:0	Gamma_table B30 value.
61h	<b>Gamma_B31</b>	<b>7:0</b>	<b>Default : 0d247</b> <b>Access : R/W</b>
	Gamma_B31	7:0	Gamma_table B31 value.
62h	<b>Gamma_B32</b>	<b>7:0</b>	<b>Default : 0d255</b> <b>Access : R/W</b>

### Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)

Index	Mnemonic	Bits	Description
	Gamma_B32	7:0	Gamma_table B32 value.

### Scaler Register (Bank = 00, Registers B0h ~ FFh)

#### Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description
<b>B0h</b>	<b>LINE_SHIFT</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	SEL_V_CLR	6	Select Vcounter Clear by DOWNCNT_EQ1 or EARLY_VS.
	-	5	Reserved.
	VCR_FF_MODE	4	Enable output VSYNC follow input VSYNC mode.
	FIELD_INV_VS	3	Line shift vs Field Inverse.
	LINE_SHIFT_NUM[2:0]	2:0	Line Shift Numbers.
<b>B1h</b>	<b>SYNC_CONTROL</b>	<b>7:0</b>	<b>Default : 0x08</b> <b>Access : R/W</b>
	CLK_DLY[3:0]	7:4	Output clock delay select.
	CLK_INV	3	Output Clock invert enable.
	DE_INV	2	Output DE Invert enable.
	VS_INV	1	Output VSYNC Invert enable.
	HS_INV	0	Output HSYNC Invert enable.
<b>B2h</b>	<b>SYNC_SEL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:4	Reserved.
	SEL_VDE	3	Select VDE output to VSYNC pin.
	SEL_HDE	2	Select HDE output to HSYNC pin.
	DATA_SKEW	1:0	Bus data Skew select.
<b>B3h ~ BFh</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
<b>C0h</b>	<b>HSPRDL_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	HSPRDL[7:0]	7:0	Number of system clock count at 512 HSYNCs.
<b>C1h</b>	<b>HSPRDL_M</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	HSPRDL[15:8]	7:0	Number of system clock count at 512 HSYNCs.
<b>C2h</b>	<b>HSPRDL_H</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	HSPRDL[23:16]	7:0	Number of system clock count at 512 HSYNCs.
<b>C3h</b>	<b>YCDLYCTL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>



**Scaler Register (Bank=00, Registers B0h ~ FFh)**

Index	Mnemonic	Bits	Description
	LNBF4_MD	7	Four Line Buffer Mode.
	VSD_PIPE	6	VSD Pipe select. 0: Original. 1: Early pipe 2 cycle.
	-	5:3	Reserved.
	YC_DLY_CTL	2:0	YC Delay Control. 000: Normal. 001: Y early 1 cycle. 010: Y early 2 cycles. 011: Y early 3 cycles. 100: Normal. 101: C early 1 cycle. 110: C early 2 cycles. 111: C early 3 cycles.
<b>C4h</b>	<b>VTOTAL_MAX_L</b>	<b>7:0</b>	<b>Default : 0xFF</b> <b>Access : R/W</b>
	TOTAL_MAX[7:0]	7:0	Vertical Max Total (lower 8 bits).
<b>C5h</b>	<b>VTOTAL_MAX_H</b>	<b>7:0</b>	<b>Default : 0x07</b> <b>Access : R/W</b>
	-	7:3	Reserved.
	TOTAL_MAX[10:8]	2:0	Vertical Max Total (higher 3 bits).
<b>C6h ~ C7h</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
<b>C8h</b>	<b>ATGCTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	MAXR (RO)	7	Max value flag for Red channel (read only). 0: Normal. 1: Max value (255) value when AGR = 0. Output over max value (255) when AGR = 1.
	MAXG (RO)	6	Max value flag for Green channel (read only). 0: Normal. 1: Max value (255) value when AGR = 0. Output over max value (255) when AGR = 1.
	MAXB (RO)	5	Max value flag for Blue channel (read only). 0: Normal. 1: Max value (255) value when AGR = 0. Output over max value (255) when AGR = 1.
	AC_EN	4	ADC Calibration Enable. 0: Disable. 1: Enable.

**Scaler Register (Bank=00, Registers B0h ~ FFh)**

Index	Mnemonic	Bits	Description	
	AGR	3	Auto Gain Result selection. 0: Output has max/min value. 1: Output is overflow/underflow.	
	ATGM	2	Auto Gain Mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATGE = 0).	
	ATGR (RO)	1	Auto Gain Result Ready. 0: Result not ready. 1: Result ready.	
	ATGE	0	Auto Gain Function Enable. 0: Disable. 1: Enable.	
<b>C9h</b>	<b>ATGST</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : R/W</b>
	VCLP	7	Video auto gain mode. 0: RGB mode. 1: YPbPr Mode.	
	-	6	Reserved.	
	CALR (RO)	5	Calibration value flag for Red channel. 0: Normal. 1: Calibration result (needs to increase offset) when ACE=1.	
	CALG (RO)	4	Calibration value flag for Green channel. 0: Normal. 1: Calibration result (needs to increase offset) when ACE=1.	
	CALB (RO)	3	Calibration value flag for Blue channel. 0: Normal. 1: Calibration result (needs to increase offset) when ACE=1.	
	MINR (RO)	2	Min value flag for Red channel. 0: Normal. 1: Min value (0) present when AGR = 0, ACE = 0. Output under min value (0) when AGR = 1, ACE = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	MING (RO)	1	Min value flag for Green channel. 0: Normal. 1: Min value (0) present when AGR = 0, ACE = 0. Output under min value (0) when AGR = 1, ACE = 0. Calibration result (needs to decrease offset) when ACE = 1.	

**Scaler Register (Bank=00, Registers B0h ~ FFh)**

Index	Mnemonic	Bits	Description
	MINB (RO)	0	Min value flag for Blue channel. 0: Normal. 1: Min value (0) present when AGR = 0, ACE = 0. Output under min value (0) when AGR = 1, ACE = 0. Calibration result (needs to decrease offset) when ACE = 1.
<b>CAh</b>	<b>ATFCHSEL</b>	<b>7:0</b>	<b>Default: 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	ATPCHSEL[1:0]	5:4	Auto Phase R/G/B channel select 00: R/G/B 3 channels 01: only R channel 10: only G channel 11: only B channel
	-	3	Reserved.
	ATGCHSEL[2:0]	2:0	Auto Gain R/G/B channel min/max value select. 000: R min value 001: G min value 010: B min value 011: R max value 100: G max value 101: B max value 11x: Reserved
<b>CBh</b>	<b>ATOCTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	JITLR	7	Jitter function Left / Right result for 86h and 87h. 0: Left result. 1: right result.
	JITS	6	Jitter Software clear. 0: Not clear. 1: Clear.
	-	5	Reserved.
	JITM	4	Jitter function Mode. 0: Update every frame. 1: Keep the history value.
	JITR	3	Jitter function Result (Read Only). 0: No jitter. 1: Jitter present.
	ATOM	2	Auto position function Mode. 0: Update every frame. 1: Keep the history value.

### Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description
	ATOR	1	Auto position result Ready (Read Only). 0: Result ready. 1: Result not ready.
	ATOE	0	Auto position function Enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.
<b>CCh</b>	<b>AOVDV</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	AOVDV[3:0]	7:4	Auto position Valid Data Value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. ... .. 1111: Valid if data >= 1111 0000.
	-	3:0	Reserved.
<b>CDh</b>	<b>ATGVALUE (RO)</b>	<b>7:0</b>	<b>Default: -</b> <b>Access : RO</b>
	ATGVALUE[7:0]	7:0	Auto Gain result based on 7Ah[2:0].
<b>CEh</b>	<b>AOVST-L (RO)</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	AOVST [7:0]	7:0	Auto position detected result Vertical Starting point.
<b>CFh</b>	<b>AOVST-H (RO)</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-	7:3	Reserved.
	AOVST[10:8]	2:0	See description for AOVST [7:0].
<b>D0h</b>	<b>AOHST-L (RO)</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	AOHST[7:0]	7:0	Auto position detected result Horizontal Starting point.
<b>D1h</b>	<b>AOHST-H (RO)</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : DB</b>
	-	7:3	Reserved.
	SPRGST[10:8]	2:0	Image horizontal sample start point, count by input dot clock.
<b>D2h</b>	<b>AOVEND-L (RO)</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	AOVEND[7:0]	7:0	Auto position detected result Vertical End point.
<b>D3h</b>	<b>AOVEND-H (RO)</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-	7:3	Reserved.
	AOVEND[10:8]	2:0	See description for AOVEND[7:0].
<b>D4h</b>	<b>AOHEND-L (RO)</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	AOHEND[7:0]	7:0	Auto position detected result Horizontal End point.

**Scaler Register (Bank=00, Registers B0h ~ FFh)**

Index	Mnemonic	Bits	Description	Access
<b>D5h</b>	<b>AOHEND-H (RO)</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	-	7:4	Reserved.	
	AOHEND[11:8]	2:0	See description for AOHEND[7:0].	
<b>D6h</b>	<b>JLR-L (RO)</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	JLR[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_7Bh[7].	
<b>D7h</b>	<b>JLR-H (RO)</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	-	7:3	Reserved.	
	JLR[10:8]	2:0	See description for JLR[7:0].	
<b>D8h</b>	<b>ANRF</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	-	7:6	Reserved.	
	HNEN	5	High level Noise reduction Enable. 0: Disable. 1: Enable.	
	BGEN	4	Background Noise reduction Enable. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	ANLV[2:0]	2:0	Auto Noise Level, 000: Noise level = 1, 001: Noise level = 2, 010: Noise level = 4, 011: Noise level = 8, 100: Noise level = 9, 101: Noise level = 10, 110: Noise level = 12, 111: Noise level = 16.	
<b>D9h</b>	<b>ATPGTH</b>	<b>7:0</b>	<b>Default : 0x01</b>	<b>Access : R/W</b>
	ATPGTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATPV3 when ATPN4 = 0.	
<b>DAh</b>	<b>ATPTTH</b>	<b>7:0</b>	<b>Default : 0x10</b>	<b>Access : R/W</b>
	ATPTTH[7:0]	7:0	Auto Phase Text Threshold for ATPV4.	
<b>DBh</b>	<b>ATPCTRL</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	ATP_FLTRMD	7	0: Disable auto-position filter mode. 1: Enable auto-position filter mode.	
	GRY (RO)	6	Gray scale detect (read only).	

### Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
	TXT (RO)	5	Text detect (read only).	
	APMASK[2:0]	4:2	Nose Mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit. 110: Mask 6 bit. 111: Mask 7 bit.	
	ATPR (RO)	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.	
	ATPE	0	Auto Phase function Enable. 0: Disable. 1: Enable.	
<b>DCh</b>	<b>ATPV1 (RO)</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	ATPVALUE[7:0]	7:0	Auto Phase Value.	
<b>DDh</b>	<b>ATPV2 (RO)</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	ATPVALUE[15:8]	7:0	See description for ATPVALUE[7:0].	
<b>DEh</b>	<b>ATPV3 (RO)</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	ATPVALUE[23:16]	7:0	See description for ATPVALUE[7:0].	
<b>DFh</b>	<b>ATPV4 (RO)</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	ATPVALUE[31:24]	7:0	See description for ATPVALUE[7:0].	
<b>E0h</b>	<b>PDMD0</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	GCLK[1:0]	7:6	Gated Clock for SRAM. 00: Normal. 01: V Blank. 10: H Blank and V Blank. 11: Reserved.	
	AUXCLK_GAT	5	0: Enable MVD MCU-support Clock. 1: Disable MVD MCU-support Clock.	
	CMBCLK_GAT	4	0: Enable MVD comb-filter Clock. 1: Disable MVD comb-filter Clock.	
	-	3	Reserved.	
	EOCLK_INV	2	External OSD sample Clock Inverting.	

**Scaler Register (Bank=00, Registers B0h ~ FFh)**

Index	Mnemonic	Bits	Description
	IDCLK_INV	1	Scaler input sample Clock Inverting.
	FSCCLK_INV	0	Sub-carrier Clock Inverting.
<b>E1h</b>	<b>PDMD1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	PDALL	7	All chip power down.
	BIUCLK_GAT	6	0: Enable register interface clock. 1: Disable register interface clock.
	OSDCLK_GAT	5	0: Enable OSD clock. 1: Disable OSD clock.
	PCCLK_GAT	4	0: Enable CRT output support clock. 1: Disable CRT output support clock.
	ADCCLK_GAT	3	0: Enable 3-channel ADC digital clock. 1: Disable 3-channel ADC digital clock.
	VDCLK_GAT	2	0: Enable CCIR and MVD interface clock. 1: Disable CCIR and MVD interface clock.
	IDCLK_GAT	1	0: Enable scaler clock. 1: Disable scaler clock.
	FSCCLK_GAT	0	0: Enable MVD digital front-end clock. 1: Disable MVD digital front-end clock.
<b>E2h</b>	<b>SWRST0</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	REGR	7	Register Reset. 0: Normal operation. 1: Reset Register.
	ADCR	6	ADC Reset. 0: Normal operation. 1: Reset ADC.
	IPR	5	Digital Input Port Reset. 0: Normal operation. 1: Reset.
	OP1R	4	Scaler Reset. 0: Normal operation. 1: Reset.
	OP2R	3	Display Port Reset. 0: Normal operation. 1: Reset.
	-	2	Reserved.

**Scaler Register (Bank=00, Registers B0h ~ FFh)**

Index	Mnemonic	Bits	Description
	OSDR	1	Internal OSD Reset. 0: Normal operation. 1: Reset internal OSD.
	SWR	0	Software Reset (reset All digital core except system registers). 0: Normal operation. 1: Reset.
<b>E3h</b>	<b>SWRST1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	VFER	7	Video Decoder Front End Reset. 0: Normal operation. 1: Reset.
	VCFR	6	Video Decoder Comb Filter Reset. 0: Normal operation. 1: Reset.
	MCUR	5	Embedded MCU Reset. 0: Normal operation. 1: Reset.
	MCUR	4	GMC digital tune Reset. 0: Normal operation. 1: Reset.
	-	3:0	Reserved.
<b>E4h</b>	<b>ISOVRD</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SL	7	Shift Line. 0: Shift line method 0. 1: Shift line method 1 for interlace mode.
	CSHS	6	HSYNC in coast. 0: HSYOUT (recommended). 1: Re-shaped HSYNC.
	UVSP	5	User defined input VSYNC Polarity, active when IVSJ =1. 0: Active low. 1: Active high.
	IVSJ	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (UVSP).
	UHSP	3	User defined input HSYNC Polarity, active when IVSJ =1. 0: Active low. 1: Active high.



### Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description
	IHSJ	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (UHSP).
	UINT	1	User defined non-interlace/interlace, active when INTJ = 1. 0: Non-interlace. 1: Interlace.
	INTJ	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (UINT).
<b>E5h</b>	<b>MDCTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	IP_TEST_MD	7:6	IP Test-bus selection.
	VERR	5	Video CCIR656 Error correct. 0: Disable. 1: Enable.
	Field_ABSMD	4	Field Position Absolute Value Mode.
	VFIV	3	Video Field Inversion. 0: Normal. 1: Invert.
	VEXF	2	Video External Field. 0: Use result of internal circuit detection. 1: Use external field.
	INTF	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.
	IFI	0	Interlace Field Inverting. 0: Normal. 1: Invert.
<b>E6h</b>	<b>HSPW (RO)</b>	<b>7:0</b>	<b>Default : -</b> <span style="float: right;"><b>Access : RO</b></span>
	HS_PW	7:0	HS Pulse Width
<b>E7h</b>	<b>VFREE</b>	<b>7:0</b>	<b>Default : 0x00</b> <span style="float: right;"><b>Access : R/W</b></span>
	AUTOOPCOAST_CLR	7	Set Auto-Coast-for-output status.
	AUTOOPCOAST	6	Enable Auto-Coast-for-output.
	MIN_VTT[5:0]	5:0	Minimum VTT to free-run.
<b>E8h</b>	<b>HSTOL</b>	<b>7:0</b>	<b>Default : 0x05</b> <span style="float: right;"><b>Access : R/W</b></span>
	VS2HS (RO)	7	Input VSYNC too close to input HSYNC.
	LN4_DETMD	6	4 Line Detect Mode for Hs, DE.

### Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description
	HSTOL[5:0]	5:0	HSYNC Tolerance. 5: Default value.
<b>E9h</b>	<b>VSTOL</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	AUTONOSIGNAL_CLR	7	Set Auto-No-Signal status.
	AUTONOSIGNAL	6	Enable Auto-No-Signal function.
	HTT_FILTERMD	5	HTT Filter Mode.
	HVTT_LOSE_MD	4	HVTT Lose Mode. 0: Original. 1: New by WDT sample.
	VS_TOL[3:0]	3:0	VSYNC Tolerance. 1: Default value.
<b>EAh</b>	<b>HSPRD_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	HSPRD[7:0]	7:0	Input Horizontal Period, count by reference clock.
<b>EBh</b>	<b>HSPRD_H</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-	7:5	Reserved.
	HSPRD[12:8]	4:0	See description for HSPRD[7:0].
<b>ECh</b>	<b>VTOTAL_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	VTOTAL[7:0]	7:0	Input Vertical Total Length, count by HSYNC.
<b>EDh</b>	<b>VTOTAL_H</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-	7:3	Reserved.
	VTOTAL[10:8]	2:0	See description for VTOTAL[7:0].
<b>EEh</b>	<b>PDMD2</b>	<b>7:0</b>	<b>Default : 0x60</b> <b>Access : RW</b>
	MCUCLK_SEL	7	MCU Clock Source Select. 0: XTAL. 1: MPLL divided.
	MCUDIV	6:4	MCU Clock divided by MPLL. 000: 4. 001: 6. 010: 8. 011: 10. 100: 12. 101: 14. 110: 16.
	-	3:1	Reserved.

**Scaler Register (Bank=00, Registers B0h ~ FFh)**

Index	Mnemonic	Bits	Description
	CC_GAT	0	Comb Clock Gating. 1: Gating mode. 0: No gating.
<b>EFh</b>	<b>STATUS2 (RO)</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	HTT_CHG_CS	7	Htotal change in CSOG.
	-	6	Reserved.
	STD_PAL	5	0: NTSC. 1: PAL.
	CSD	4	CSYNC Detected status. 0: Input is not CSYNC. 1: Input is detected as CSYNC.
	INTM	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.
	INTF	2	Input odd/even Field detecting result by this chip. 0: Even. 1: Odd.
	IHSP	1	Incoming input HSYNC Polarity detecting result by this chip. 0: Active low. 1: Active high.
	IVSP	0	Incoming input VSYNC Polarity detecting result by this chip. 0: Active low. 1: Active high.
<b>F0h</b>	<b>CHIP_ID</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : RO</b>
	CHIP_ID[7:0]	7:0	Chip id is 70h
<b>F1h</b>	<b>CHIP_VERSION</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : RO</b>
	CHIP_VER[7:0]	7:0	Version is 01h
<b>F2h ~ F3h</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
<b>F4h</b>	<b>TRISTATE</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	OBBUS_TRI	4	Output bus Tristate.
	VS_TRI	3	Output VSYNC Tristate.
	HSY_TRI	2	Output HSYNC Tristate.
	DE_TRI	1	Output DE Tristate.

### Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description
	CLK_TRI	0	Output CLK Tristate.
<b>F7h ~ FFh</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.

### Analog Register (Bank = 01)

Analog Register (Bank = 01)			
Index	Name	Bits	Description
<b>01h</b>	<b>DBFC</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:1	Reserved.
	DBVB	0	Double Buffer load at Vertical Blanking. 0: Disable. 1: Enable.
<b>02h</b>	<b>PLLDIVM</b>	<b>7:0</b>	<b>Default : 0x69</b> <b>Access : R/W</b>
	PLLDIV[11:4]	7:0	PLL Divider ratio. ADC PLL will multiply the horizontal line frequency by PLLDIV[11:0]+3 to generate the ADC sampling clock.
<b>03h</b>	<b>PLLDIVL</b>	<b>7:0</b>	<b>Default : 0x50</b> <b>Access : R/W</b>
	PLLDIV[3:0]	7:4	PLL Divider ratio. ADC PLL will multiply the horizontal line frequency by PLLDIV[11:0]+3 to generate the ACD sampling clock. PLLDIV[11:0] default value: 1685 (1688-3).
		3:0	Reserved.
<b>04h</b>	<b>RGAIN_ADC</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	RGAIN_ADC[7:0]	7:0	ADC Red channel Gain adjust.
<b>05h</b>	<b>GGAIN_ADC</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	GGAIN_ADC[7:0]	7:0	ADC Green channel Gain adjust.
<b>06h</b>	<b>BGAIN_ADC</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	BGAIN_ADC[7:0]	7:0	ADC Blue channel Gain adjust.
<b>07h</b>	<b>ROFFS_ADC</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	ROFFS_ADC[7:0]	7:0	ADC Red channel Offset adjust.
<b>08h</b>	<b>GOFFS_ADC</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	GOFFS_ADC[7:0]	7:0	ADC Green channel Offset adjust.
<b>09h</b>	<b>BOFFS_ADC</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>

**Analog Register (Bank = 01)**

Index	Name	Bits	Description
	BOFFS_ADC[7:0]	7:0	ADC Blue channel Offset adjust.
<b>0Ah</b>	<b>CLPACE</b>	<b>7:0</b>	<b>Default : 0x05</b> <b>Access : R/W</b>
	CLPACE	7:0	Clamp Placement based on ADC clock.
<b>0Bh</b>	<b>CLDUR</b>	<b>7:0</b>	<b>Default : 0x05</b> <b>Access : R/W</b>
	CLDUR	7:0	Clamp Duration based on ADC clock.
<b>0Ch</b>	<b>GCTRL</b>	<b>7:0</b>	<b>Default : 0x82</b> <b>Access : R/W</b>
	HSP	7	Input HSYNC Polarity. 0: Active low. 1: Active high.
	ECLK	6	External Clock. 0: ADC clock from internal ADC PLL. 1: ADC clock from external clock.
	HSLE	5	HS Lock Edge. Determines which edge of HSYNC the ADC PLL will lock to, assuming HSP is set correctly. 0: Leading edge of HSYNC. 1: Trailing edge of HSYNC.
	CLPE	4	Clamp reference Edge. 0: Trailing edge of HSYNC. 1: Leading edge of HSYNC.
	CCDIS	3	Disable PLL watchdog timer. 0: Always enable clamp. 1: Disable clamp during active coast.
	WDIS	2	Disable watchdog timer. 0: Enable PLL watchdog timer. A watchdog timer is used to reset the ADC PLL when the PLL remains much higher than PLLDIV*HSYNC_FREQ for a predetermined period. See WDTOL (Register 30h). 1: Disable PLL watchdog timer (should only be used when DPL_S=0).
	CSTP	1	Coast Polarity. 0: Active low. 1: Active high.
	-	0	Reserved.
<b>0Dh</b>	<b>BWCOEF</b>	<b>7:0</b>	<b>Default : 0x85</b> <b>Access : R/W</b>

<b>Analog Register (Bank = 01)</b>			
<b>Index</b>	<b>Name</b>	<b>Bits</b>	<b>Description</b>
	BWCOEF[7:6]	7:6	Damping coefficient mode control. 00: Default value – backward compatibility mode. 01: Reserved. 10: Automatic DCOEF control (recommended mode). 11: Reserved.
	BWCOEF[5:0]	5:0	PLL loop filter control.
<b>0Eh</b>	<b>FCOEF</b>	<b>7:0</b>	<b>Default : 0x09</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	FREQCOEF[4:0]	4:0	PLL loop filter control.
<b>0Fh</b>	<b>DCOEF</b>	<b>7:0</b>	<b>Default : 0x03</b> <b>Access : R/W</b>
		7:4	Reserved.
	DAMPCOEF[3:0]	3:0	PLL loop filter control.
<b>10h</b>	<b>CLKCTRL1</b>	<b>7:0</b>	<b>Default : 0x08</b> <b>Access : R/W</b>
	-	7	Reserved.
	STAT[2]	6	Status select; selects internal PLL status values to read from register 1Eh.
	PHASEADC	5:0	Clock Phase adjust for ADC (set to PHASECC+8).
<b>11h</b>	<b>CLKCTRL2</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	STAT[1:0]	7:6	Status select; selects 1/8 internal PLL status values to read from register 1Eh.
	PHASECC[5:0]	5:0	Clock phase adjust for ADC sampling time point; phase is adjustable between 0 and 360° in 5.6° steps.
<b>12h</b>	<b>VCOCTRL</b>	<b>7:0</b>	<b>Default : 0x15</b> <b>Access : R/W</b>
	PDGT	7	Phase digitizer frequency compensation disable.
	-	6:4	Reserved.
	SETCNT[3:0]	3:0	Setting time for ADC PLL phase detector, in ADC clock periods.
<b>13h</b>	<b>RT_CT</b>	<b>7:0</b>	<b>Default : 0xC6</b> <b>Access : R/W</b>
	TOLCN[1:0]	7:6	Watchdog maximum Count. 0: 0. 1: 4. 2: 32. 3: 127.
	IQ1LEN[2:0]	5:3	Counter for IQ from high to low.
	IQ0LEN[2:0]	2:0	Counter for IQ from low to high.
<b>14h</b>	<b>SOG_LVL</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>

**Analog Register (Bank = 01)**

Index	Name	Bits	Description
	RMID	7	Middle clamp of Red Channel. 0: Disable. 1: Enable (used when YPbPr input).
	BMID	6	Middle clamp of Blue Channel. 0: Disable. 1: Enable (used when YPbPr input).
	-	5:0	Reserved.
<b>15h</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
<b>16h</b>	<b>DITHCTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	DIT_TOG_LEN4	7	0: Select Length 2 Toggle Loop. 1: Select Length 4 Toggle Loop.
	DIT_TOG_R	6	1: Enable ADC R Toggle Dither.
	DIT_TOG_G	5	1: Enable ADC G Toggle Dither.
	DIT_TOG_B	4	1: Enable ADC B Toggle Dither.
	DIT_LVL_CAL	3:2	Select ADC Dither Level for CAL.
	DIT_LVL	1:0	Select ADC Dither Level for display.
<b>17h</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
<b>18h</b>	<b>CALEN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CALG_EN	7	ADC gain auto-cal function enable. 0: Disable. 1: Enable.
	CALG_UPD	6	Auto update GAIN enable. 0: Disable. 1: Enable.
	TRIG_CALG	5	Trigger gain calibration enable. 0: Disable. 1: Enable.
	CALO_EN	4	ADC offset auto-cal function enable. 0: Disable. 1: Enable.
	CALO_UPD	3	Auto update offset enable. 0: Disable. 1: Enable.

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	TRIG_CALO	2	Trigger offset calibration enable. 0: Disable. 1: Enable.
	CAL_CHAN	1:0	Select manual mode calibration channel. 00: R. 01: G. 10: B. 11: Reserved.
<b>19h</b>	<b>CALCTL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	CAL_UPD_HS	5	Update CAL value during HS. 0: Disable. 1: Enable.
	CAL_ONESHOTZ	4	CAL on one-shot loop/real time. 0: CAL on one-shot loop time. 1: CAL on one-shot real time.
	CAL_STOP	3	Stop (halt) auto offset calibration. 0: Disable. 1: Enable.
	CAL_MODE2	2	Auto-stop calibration after 128 frames. 0: Enable. 1: Disable.
	BYPASSDOUT	1	Bypass DOUT during CAL. 0: Disable. 1: Enable.
	CAL_EDGE	0	CAL from HS leading/trailing edge. 0: CAL from HS leading edge. 1: CAL from HS trailing edge.
<b>1Ah</b>	<b>CALSMP</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	STATUS_SEL[2:0]	7:5	Select status of STATUS_CAL. 000: {CAL_DOUT[5:0], 1'b0, CAL_DONE}. 001: Calibrated R offset. 010: Calibrated G offset. 011: Calibrated B offset. 100: CAL_DOUT[13:6]. 101: Digital Offset R. 110: Digital Offset G. 111: Digital Offset B.



### Analog Register (Bank = 01)

Index	Name	Bits	Description
	SMPDLY_EN	4	Use default/SMPDLY as CAL sample delay. 0: Use internal default as CAL sample delay. 1: Use SMPDLY as CAL sample delay.
	SMPDLY	3:0	Calibration sample delay.
<b>1Bh</b>	<b>CALDUR</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CALCNT_EN	7	Use default/CALDLY-CALDUR to generate CAL pulse. 0: Use default to generate CAL pulse. 1: Use CALDLY-CALDUR to generate CAL pulse.
	CALDUR[6:0]	6:0	CAL pulse duration register.
<b>1Ch</b>	<b>CALDLY</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CALDLY[7:0]	7:0	CAL pulse delay register.
<b>1Dh</b>	<b>STATUS_CAL</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	Note: Calibration status is read based on STATUS_SEL[2:0] (Bank 01, Reg_1Ah[7:5]).		
	STATUS_SEL[2:0]		
	7:5		Reserved.
	4		CAL_DOUT[13:6].
	3		CAL_OFFSB.
	2		CAL_OFFSG.
	1		CAL_OFFSR.
	0		{CAL_DOUT[5:0], 1'b0, CAL_DONE}.
<b>1Eh</b>	<b>STATUS_PLL</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	Note: PLL status is read based on STAT[2:0] (Bank 01, Reg_10h[6] and Bank 02, Reg-11h[76]).		
	STAT[2:0]		
	000	7	[2'd0, SAR_MIN].
		6	{2'd0, SAR_MAX}.
		5	{SAR_AVG[19:12].
		4	{1'b0, ICAI_s[6:0]}.
		3	{1'b0, SAR_s[6:0]}.
		2	{FREQCTRL[15:8]}.
		1	{FREQCTRL[23:16]}.
		0	{LOCK, IQ, SLOW, FAST, FREERUN, 3'b000}.
<b>1Fh ~ 22h</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
<b>23h</b>	<b>FPLL_STATUS</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	FPLL_STATUS[7:0]	7:0	FPLL Status.
<b>24h</b>		<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	-	7:5	Reserved.
	FPLL_MD	4	FPLL Mode selection. 0: CVBS. 1: RGB.
	-	3:0	Reserved.
<b>25h</b>	<b>FPLL_DIVN</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:4	Reserved.
	FPLL_DIVN[3:0]	3:0	FPLL Feed back Divider. 0000: Divide by 1. 0001: Divide by 2. 0010: Divide by 3. ... 1111: Divide by 16.
<b>26h ~ 28h</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:5	Reserved.
<b>29h</b>	<b>ADC_REG</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	ADC_IMD	4:3	Set ADC total current.
	RENC_ADC	2	RGB mode: set to 0/CVBS mode: set to 1.
	GENC_ADC	1	RGB mode: set to 0/CVBS mode: set to 1.
	BENC_ADC	0	RGB mode: set to 0/CVBS mode: set to 1.
<b>2Ah ~ 2Bh</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
<b>2Ch</b>	<b>RGB_BW_SEL1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	-	5:4	Reserved.
	-	3	Reserved.

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	R_BW[2:0]	2:0	R-channel input filter BW select. 000: 200 MHz. 001: 165 MHz. 010: 130 MHz. 011: 87 MHz. 100: 65 MHz. 101: 30 MHz. 110: 10 MHz. 111: 6 MHz.
2Dh	<b>RGB_BW_SEL2</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	G_BW[2:0]	6:4	G-channel input filter BW select.
	-	3	Reserved.
	B_BW[2:0]	2:0	B-channel input filter BW select.
2Eh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
2Fh	<b>ADC_MUX</b>	<b>7:0</b>	<b>Default :</b> <b>Access :</b>
	-	7:6	Reserved.
	MUX[5:0]	5:0	See ADC MUX TABLE.
30h ~ 9Bh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
9Ch	<b>ADC_MD_CTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	ADC_DCTRL	7:6	Reserved for ADC DCTRL.
	GSHIFT_R	5	1: Enable ADC R Gain Range Shift for VD Mode.
	GSHIFT_G	4	1: Enable ADC G Gain Range Shift for VD Mode.
	GSHIFT_B	3	1: Enable ADC B Gain Range Shift for VD Mode.
	ADC_VCTRL	2:0	ADC Voltage Control (Recommend Setting = 3'b011).
9Dh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
9Eh	<b>CAL_CTRL3</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	CAL_STSWEN	6	1: Enable Write to Internal CAL Registers through STATUS_CAL.

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	CAL_SWOV	5:4	00: Normal Mode. 01: Switch ADC Input to Offset CAL Reference Voltage. 10: Reserved. 11: Reserved.
	CAL_HOLD	3	1: Hold Current CAL Result for Display.
	CAL_INPUT	2	0: CAL to Internal Offset Reference Voltage. 1: CAL to ADC Input.
	CAL_HYS	1	1: Enable CAL Update Hytheresis.
	DOFFS_EN	0	1: Enable Digital Offset Adjustment.
<b>9Fh</b>	<b>ADCTOUT</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:4	Reserved.
	ADCTOUT_SYNC	3	1: Enable ADC Test Out Sync to CKEXT.
	ADCTOUT_DIV	2:0	Select ADC Test Out Decimation Ratio (1~8).
<b>A0h</b>	<b>RG_DRV</b>	<b>7:0</b>	<b>Default : 0x55</b> <b>Access : R/W</b>
	G[7:6]_DRV[1:0]	7:6	Pad G[7:4] Driving select.
	G[5:4]_DRV[1:0]	5:4	Pad G[3:0] Driving select.
	R[3:2]_DRV[1:0]	3:2	Pad R[7:4] Driving select.
	R[1:0]_DRV[1:0]	1:0	Pad R[3:0] Driving select.
<b>A1h</b>	<b>RG_DRV</b>	<b>7:0</b>	<b>Default : 0x55</b> <b>Access : R/W</b>
	HS_DRV[1:0]	7:6	Pad Hsync Driving select.
	VS_DRV[1:0]	5:4	Pad Vsync Driving select.
	B[7:4]_DRV[1:0]	3:2	Pad B[7:4] Driving select.
	B[3:0]_DRV[1:0]	1:0	Pad B[3:0] Driving select.
<b>A2h</b>	<b>RG_DRV</b>	<b>7:0</b>	<b>Default : 0x55</b> <b>Access : R/W</b>
	PWM2_DRV[1:0]	7:6	Pad PWM2 Driving select.
	PWM1_DRV[1:0]	5:4	Pad PWM1 Driving select.
	CLK_DRV[1:0]	3:2	Pad CLK Driving select.
	DE_DRV[1:0]	1:0	Pad DE Driving select.
<b>A3h</b>	<b>EPD_R</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EPD_R[7:0]	7:0	Enable Pull Down in R channel.
<b>A4h</b>	<b>EPD_G</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EPD_G[7:0]	7:0	Enable Pull Down in G channel.
<b>A5h</b>	<b>EPD_B</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EPD_B[7:0]	7:0	Enable Pull Down in B channel.

### Analog Register (Bank = 01)

Index	Name	Bits	Description	Access
<b>A6h</b>	<b>EPD_R</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	-	7:6	Reserved.	
	EPD_PWM2	5	Enable pull down in PWM2 pad.	
	EPD_PWM1	4	Enable pull down in PWM2 pad.	
	EPD_CLK	3	Enable pull down in CLK pad.	
	EPD_DE	2	Enable pull down in DE pad.	
	EPD_HS	1	Enable pull down in HSYNC pad.	
EPD_VS	0	Enable pull down in VSYNC pad.		
<b>A7h ~ AAh</b>	-	<b>7:0</b>	<b>Default : -</b>	<b>Access : -</b>
	-	7:0	Reserved.	
<b>ABh</b>	<b>VDAC_ADJ2</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	-	7:5	Reserved.	
	ED[4:0]	4:0	Testing control for voltage DAC.	
<b>ACh ~ C9h</b>	-	<b>7:0</b>	<b>Default : -</b>	<b>Access : -</b>
	-	7:0	Reserved.	
<b>CAh</b>	<b>POL_SET0</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	POL_OUT_INV	7	POL Output Invert.	
	POL_TP	6:0	POL Transition Point.	
<b>CBh</b>	<b>POL_SET1</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	-	7:5	Reserved.	
	POL_SEL	4	0: VSYNC Frequency POL. 1: HSYNC Frequency POL.	
	POL_PVI_10IN	3	POL Output to SEQ_MOD Pin if EFh[7] = 0.	
-	2:0	Reserved.		
<b>CCh</b>	<b>SCAL_ACT</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	-	7:6	Reserved.	
	TC_CLK_DIV2	5	TC Clock Divide 2.	
	-	4	Reserved.	
	LINE_ACT_D1L	3	Line Active Delay One Line time.	
	LINE_ACT_EN	2	TCON Line_Extract Mode work with Digital V_Scaling.	
	-	1:0	Reserved.	
<b>CDh</b>	<b>GPO_OEV2_WIDTH</b>	<b>7:0</b>	<b>Default : 0x54</b>	<b>Access : R/W</b>
	GPO_OEV2_DIS	7	OEV2 Disable.	

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	GPO_OEV2_WIDTH [6:0]	6:0	OEV2 Pulse Width.
CEh	<b>GPO_OEV3_WIDTH</b>	<b>7:0</b>	<b>Default : 0x54</b> <b>Access : R/W</b>
	GPO_OEV3_DIS	7	OEV3 Disable.
	GPO_OEV3_WIDTH [6:0]	6:0	OEV3 Pulse Width.
CFh	<b>GPO_OEV_DELTA</b>	<b>7:0</b>	<b>Default : 0x54</b> <b>Access : R/W</b>
	-	7:4	Reserved.
	GPO_OEV_DELTA[3:0]	3:0	Adjust OEV distance.
D0h	<b>PTC_MODE1</b>	<b>7:0</b>	<b>Default : 0x8C</b> <b>Access : R/W</b>
	TC_MD	7	TC signal output enable. 0: Disable set low. 1: Enable.
	OEV_DELTA_EN	6	OEV distance adjust Enable.
	DOU_EXTR_MD[1:0]	5:4	00: Normal mode. 01: Paranoia extract mode. 10: Full extract mode. 11: Line duplicate mode.
	FRAME_INV_EN	3	0: Disable. 1: Enable.
	EARLY_VS	2	Early vs.
	FIELD_SEL	1	Select field inverse from IP.
	LN_SHIFT	0	Field Line Shift enable.
D1h	<b>PTC_MODE2</b>	<b>7:0</b>	<b>Default : 0x3E</b> <b>Access : R/W</b>
	TCCLK_CONF[1:0]	7:6	7: 13 CLK swap. 6: 3 CLK inverse.
	SEQ_MD	5	0: Single clock output mode. 1: Three clock output mode.
	TCCLK_MD	4	Select 3TC CLK or 1 TC CLK.
	STHLR_SEL	3	0: STHR. 1: STHL.
	STVLR_SEL	2	0: STVR. 1: STVL.
	L_R	1	0: L_R equal 0. 1: L_R equal 1.

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	U_D	0	0: U_D=0. 1: U_D=1.
<b>D2h</b>	<b>PTC_MODE3</b>	<b>7:0</b>	<b>Default : 0x84</b> <b>Access : R/W</b>
	SET_TCCLK23_VALUE	7	Set TCCLK23 High/Low.
	LG_MD	6	LG_panel Mode enable.
	DF_EXT_LN	5	Different frame, Different Extract Line mode. 0: Disable. 1: Enable.
	LN_DUP_MD[1:0]	4:3	Duplicate 2/3 Line Mode. 4: OEV3 enable. 3: OEV2 enable.
	FIELD_IN_SEL	2	Select Field source from OP2 or free-run.
	LINE_INV_DIS	1	Line Inverse Disable. 0: Enable. 1: Disable.
	FRP_VCOM_INV	0	VCOM Inverse to FRP.
<b>D3h</b>	<b>LN_EXTR_CNT_LMT</b>	<b>7:0</b>	<b>Default : 0xDD</b> <b>Access : R/W</b>
	LN_EXTR_CNT_LMT2	7:4	Line Extract/duplicate Counter 2.
	LN_EXTR_CNT_LMT1	3:0	Line Extract/duplicate Counter 1.
<b>D4h</b>	<b>LN_EXTR_SET1_H</b>	<b>7:0</b>	<b>Default : 0x2F</b> <b>Access : R/W</b>
	LN_EXTR_SET1[7:0]	7:0	Line Extract/duplicate set 1 High byte.
<b>D5h</b>	<b>LN_EXTR_SET1_L</b>	<b>7:0</b>	<b>Default : 0xEF</b> <b>Access : R/W</b>
	LN_EXTR_SET1[15:8]	7:0	Line Extract/duplicate set 1 Low byte.
<b>D6h</b>	<b>LN_EXTR_SET2_H</b>	<b>7:0</b>	<b>Default : 0x1F</b> <b>Access : R/W</b>
	LN_EXTR_SET2[7:0]	7:0	Line Extract/duplicate set 2 High byte.
<b>D7h</b>	<b>LN_EXTR_SET2_L</b>	<b>7:0</b>	<b>Default : 0xE7</b> <b>Access : R/W</b>
	LN_EXTR_SET2[15:8]	7:0	Line Extract/duplicate set 2 Low byte.
<b>D8h</b>	<b>EXTR_STT_LN1</b>	<b>7:0</b>	<b>Default : 0x02</b> <b>Access : R/W</b>
	EXTR_STT_LN1[7:0]	7:0	Line Extract/duplicate Start Line 1.
<b>D9h</b>	<b>EXTR_END_LN1</b>	<b>7:0</b>	<b>Default : 0x30</b> <b>Access : R/W</b>
	EXTR_END_LN1[7:0]	7:0	Line Extract/duplicate End Line 1.
<b>DAh</b>	<b>EXTR_STT_LN2</b>	<b>7:0</b>	<b>Default : 0x50</b> <b>Access : R/W</b>
	EXTR_STT_LN2[7:0]	7:0	Line Extract/duplicate Start Line 2.
<b>DBh</b>	<b>EXTR_END_LN2</b>	<b>7:0</b>	<b>Default : 0x77</b> <b>Access : R/W</b>

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	EXTR_END_LN2[7:0]	7:0	Line Extract/duplicate End Line 2.
DCh	<b>GPO_FRP_TRAN</b>	<b>7:0</b>	<b>Default : 0x13</b> <b>Access : R/W</b>
	OUT_INV	7	Output Inverse.
	GPO_FRP_TRAN_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_FRP_TRAN[4:0]	4:0	FRP Transition position.
DDh	<b>GPO_STH_STT</b>	<b>7:0</b>	<b>Default : 0x46</b> <b>Access : R/W</b>
	OUT_INV	7	Output Inverse.
	GPO_STH_STT_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_STH_STT[4:0]	4:0	STH pulse Start position.
DEh	<b>GPO_STH_WIDTH</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	GPO_STH_WIDTH_MULT[1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_STH_WIDTH [3:0]	3:0	STH pulse Width.
DFh	<b>GPO_OEH_STT</b>	<b>7:0</b>	<b>Default : 0xA3</b> <b>Access : R/W</b>
	OUT_INV	7	Output Inverse.
	GPO_OEH_STT_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_OEH_STT[4:0]	4:0	OEH pulse Start position.
E0h	<b>GPO_OEH_WIDTH</b>	<b>7:0</b>	<b>Default : 0x0B</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	GPO_OEH_WIDTH_MULT[1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.



### Analog Register (Bank = 01)

Index	Name	Bits	Description
	GPO_OEH_WIDTH [3:0]	3:0	OEH pulse Width.
<b>E1h</b>	<b>GPO_OEV_STT</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	OUT_INV	7	Output Inverse.
	GPO_OEV_STT_MMULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_OEV_STT[1:0]	4:0	OEV pulse Start.
<b>E2h</b>	<b>GPO_OEV_WIDTH</b>	<b>7:0</b>	<b>Default : 0x6D</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	GPO_OEV_WIDTH_MULT[1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_OEV_WIDTH [3:0]	3:0	OEV pulse Width.
<b>E3h</b>	<b>GPO_CKV_STT</b>	<b>7:0</b>	<b>Default : 0x2D</b> <b>Access : R/W</b>
	OUT_INV	7	Output Inverse.
	CKV_STT_MULT[1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_CKV_STT[4:0]	4:0	CKV pulse Start.
<b>E4h</b>	<b>GPO_CKV_STT2</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	CKV_STT2_MULT [1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_CKV_ST2[3:0]	3:0	CKV pulse Start 2.
<b>E5h</b>	<b>GPO_CKV_WIDTH</b>	<b>7:0</b>	<b>Default : 0x5F</b> <b>Access : R/W</b>
	-	7	Reserved.

**Analog Register (Bank = 01)**

Index	Name	Bits	Description
	CKV_WIDTH_MULT[1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_CKV_WIDTH[4:0]	4:0	CKV pulse width.
<b>E6h</b>	<b>GPO_STV_LN_TH</b>	<b>7:0</b>	<b>Default : 0x46</b> <b>Access : R/W</b>
	-	7	Reserved.
	GPO_STV_1LN	6	STV width is 1 Line.
	GPO_STV_LINE_TH	5:0	STV line position
<b>E7h</b>	<b>GPO_STV_STT</b>	<b>7:0</b>	<b>Default : 0x29</b> <b>Access : R/W</b>
	OUT_INV	7	Output Inverse.
	STV_STT_MULT[1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_STV_STT[4:0]	4:0	STV pulse Start.
<b>E8h</b>	<b>GPO_STV_WIDTH</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	STV_WIDTH_MULT [1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_STV_WIDTH [3:0]	3:0	STV pulse Width.
<b>E9h</b>	<b>GPO_OEV2_STT</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	OUT_INV	7	Output Inverse.
	OEV2_STT_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_OEV2_STT[4:0]	4:0	OEV2 pulse Start.
<b>EAh</b>	<b>GPO_OEV3_STT</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	OUT_INV	7	Output Inverse.

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	OEV3_STT_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_OEV3_STT[4:0]	4:0	OEV3 pulse Start.
<b>EBh</b>	<b>HSTT_DLY_L</b>	<b>7:0</b>	<b>Default :0x04</b> <b>Access : R/W</b>
	HSTT_DLY[7:0]	7:0	H Start Delay numbers Low byte.
<b>ECh</b>	<b>HSTT_DLY_H</b>	<b>7:0</b>	<b>Default :0xA4</b> <b>Access : R/W</b>
	EXT_DIS_RNG	7:4	Extraction start point in line extraction mode.
	-	3	Reserved.
	HSTT_DLY_EN	2	H Start Delay Enable.
	HSST_DLY[9:8]	1:0	H Start Delay numbers High byte.
<b>EDh</b>	<b>CLK_DLY_SYNCOUT</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	FRPSETH	7	Set High to Invert RGB Data when FRP Disable (BK1_D2[1]=1).
	-	6	Reserved.
	TC_GPIO_SEL	5	0: TC function. 1: GPIO function.
	OEV_MD_SEL	4	0: Normal mode. 1: Special mode.
	CLK_DLY_SEL_TC [3:0]	3:0	TCCLK Delay Select.
<b>EEh</b>	<b>GPO_CKV_END2</b>	<b>7:0</b>	<b>Default : 0x28</b> <b>Access : R/W</b>
	CKV2_EN	7	CKV2 Enable.
	CKV_END2_MULT[1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.
	GPO_CKV_END2	4:0	CKV2 End point.
<b>EFh</b>	<b>Q1H_SETTING</b>	<b>7:0</b>	<b>Default : 0x08</b> <b>Access : R/W</b>
	Q1H_ENABLE	7	Q1H output from SEQ_MODE pin, toggle point is using OEV3 signal start point.
	TCCLK_INV_MODE	6:3	0001: TCCLK invert every field. 0011: TCCLK invert when Q1H is high. 0101: TCCLK invert when Q1H and field are high. 1001: TCCLK invert when Q1H is low and field is high.

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	-	2	Reserved.
	INTOUT_OEN	1	Testmode. PAD_INTOUT output enable control. 0: Output. 1: Input.
	CLKIN_SEL	0	Testmode External Clock Select. 0: PAD_INTOUT. 1: PAD_CLKIN.
<b>F0h</b>	<b>WDT0</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	WDT_TESTMD	7	CSOG test mode for WDT counter.
	WDT_LD	6	Watch Dog Timer Load Value by SW.
	WDT_EN	5	Watch Dog Timer Enable Bit.
	-	4:0	Reserved.
<b>F1h</b>	<b>WDT1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	WDT_WIDTH	7:0	Watch Dog Timer Width.
<b>F2h</b>	<b>WRLOCK0</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	WRLOCK0	7	Register lock (work with WRLOCK1). Register access is disabled when WRLOCK0 and WRLOCK1 are HIGH. Register access is enabled when WRLOCK0 and WRLOCK1 are LOW.
	-	6:0	Reserved.
<b>F3h</b>	<b>PWMCLK</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	DB_EN	7	Double Buffer Enable. 0: Disable. 1: Enable.
	P2REN	6	PWM2 Reset every frame Enable. 0: Disable. 1: Enable.
	P1REN	5	PWM1 Reset every frame Enable. 0: Disable. 1: Enable.
	P2POL	4	PWM 2 Polarity when enhance PWM2 enable.
	EP2EN	3	Enhance PWM2 Enable. 0: Disable. 1: Enable.
	P1POL	2	PWM1 Polarity when enhance PWM1 enable.

### Analog Register (Bank = 01)

Index	Name	Bits	Description
	EP1EN	1	Enhance PWM1 Enable. 0: Disable. 1: Enable.
	PCLK	0	PWM1/2 base Clock select. 0: 14.318MHz. 1: 14.318MHz / 4.
<b>F4h</b>	<b>PWM1C</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	PWM1_POL	7	PWM1 polarity.
	PWM1_CTUN[6:0]	6:0	PWM1 Coarse adjustment.
<b>F5h</b>	<b>PWM2C</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	PWM2_POL	7	PWM2 polarity.
	PWM2_CTUN[6:0]	6:0	PWM2 Coarse adjustment.
<b>F6h</b>	<b>PWM1EPL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EPWM1P[7:0]	7:0	Enhance PWM1 Period.
<b>F7h</b>	<b>PWM1EPH</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EPWM1P[15:8]	7:0	Enhance PWM1 Period.
<b>F8h</b>	<b>PWM2EPL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EPWM2P[7:0]	7:0	Enhance PWM2 Period.
<b>F9h</b>	<b>PWM2EPH</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	EPWM2P[15:8]	7:0	Enhance PWM2 Period.
<b>FAh ~</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
<b>FFh</b>	-	7:0	Reserved.

### Video Decoder Register (Bank = 02)

Video Decoder Register (Bank = 02)			
Index	Name	Bits	Description
<b>01h</b>	<b>STATUS1</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	READBUS1	7:0	Test bus 1.
<b>02h</b>	<b>STATUS2</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	READBUS2	7:0	Test bus 2.
<b>03h</b>	<b>STATUS3</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	READBUS3	7:0	Test bus 3.
<b>04h</b>	<b>STATUS_MUX</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	READBUS_CTRL	7:0	VIPTSTMUX Address Control of READBUS1, READBUS2, and READBUS3.
05h ~ 06h	-	7:0	Default : - Access : -
	-	7:0	Reserved.
07h	<b>DSP_ADD_PRT</b>	7:0	Default : 0x00 Access : R/W
	DSP_ADD_PRT[7:0]	7:0	DSP register Address Port.
08h	<b>DSP_WDAT_PRT</b>	7:0	Default : 0x00 Access : R/W
	DSP_WDAT_PRT[7:0]	7:0	DSP register Write Data Port.
09h	<b>DSP_RDAT_PRT</b>	7:0	Default : - Access : RO
	DSP_RDAT_PRT[7:0]	7:0	DSP register Read Data Port.
10h	-	7:0	Default : - Access : -
	-	7:0	Reserved.
11h	<b>COMB_LL_EN</b>	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	APL_COMB_LL_EN	0	1: Mux to select Com Line Lock mode.
12h ~ 13h	-	7:0	Default : - Access : -
	-	7:0	Reserved.
14h	<b>SOFT_RST</b>	7:0	Default : 0x10 Access : R/W
	SOFT_RST	7	1: Softrest AFEC modules.
	-	6:0	Reserved.
15h	<b>FPGA_CTRL</b>	7:0	Default : 0xA8 Access : R/W
	FPGA_CTRL	7:0	Reserved for FPGA control.
16h	<b>REG_SOFT_RST2</b>	7:0	Default : 0x00 Access : R/W
	REG_SOFT_RST2	7:0	Reserved for HW testing.
17h	<b>CLK_CTRL</b>	7:0	Default : 0xC9 Access : R/W
	FSCPLL_MODE	7	0: External FSC Clock Mode. 1: Internal FSC Clock Mode.
	ADC_DOUBLE	6	ADC Double Sample Rate Option.
	REG_CLK_VD_VIP	5:4	00: 4 Fsc Clock on Digital. 11: 8 Fsc Clock on Digital.
	REG_VCO_TYPE	3:2	10: VCO 16 Fsc. 01: VCO 8 Fsc. 00: VCO 4 Fsc.
	REG_ADC_CLK_LAG	1:0	CLK_CC / CLK_ADC Phase Diff.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
18h	<b>CSTATE_CTRL</b>	<b>7:0</b>	<b>Default : 0x86</b> <b>Access : R/W</b>
	CTRL_MD	7:5	Default: 100b, Auto control mode.
	-	4	Reserved.
	CTRL_STATE	3:0	State Stable State Value; default: 0110b.
19h	<b>MVDET_EN</b>	<b>7:0</b>	<b>Default : 0xC0</b> <b>Access : R/W</b>
	MV_DETEC_EN	7	Microvision Detect Enable. 0: Disable. 1: Enable.
	-	6:5	Reserved.
	DSP_SYNC_ALW	4	Allow DSP to Control SYNC_FOUND.
	DSP_APL_ALW	3:2	0: Allow DSP to Control APL_FREQ_IDEAL (Center Frequency).
	-	1:0	Reserved.
1Ah	<b>SVD_EN</b>	<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>
	SVIDEO_EN	7	0: Chroma Source from CVBS-Channel Input. 1: Chroma Source from C-Channel Input.
	ADC_C_ALWY_ON	6	Chroma ADC 16Fsc-to-4Fsc Down-Sampling is Enabled.
	CLAMDMSM_CTRL[15:10]	5:0	Clamping 12-bit Control code; integer parts.
1Bh	<b>BKLV_L_FORCE1</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	DISCLAMP3	7	HW Clamping frozen 3 times if SYNC magnitude is small.
	CLMP_FREZ_ZERO	6	HW Clamping set to Zero when Frozen.
	CLAMDMSM_CTRL[9:4]	5:0	Clamping 12-bit control code; fractional parts.
1Ch	<b>BKLV_L_FORCE2</b>	<b>7:0</b>	<b>Default : 0xFF</b> <b>Access : R/W</b>
	CLMFZE_VRGE	7:0	Clamp Freeze of V Range.
1Dh	<b>VCR_VLSHT</b>	<b>7:0</b>	<b>Default : 0xFF</b> <b>Access : R/W</b>
	CLMFZE_HRGE	7:0	Clamp Freeze of H Range.
1Eh	<b>DSP_EN</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	DSP_EN_SYS	7	1: Enable SW DSP Function.
	-	6:0	Reserved.
1Fh	<b>CLMP_C_EN</b>	<b>7:0</b>	<b>Default : 0x60</b> <b>Access : R/W</b>
	CLMP_C_EN	7	2nd ADC Chroma Clamping Enable.
	CLMP_K1_INI	6:0	HW Clamping K1 when system not stable.
20h	<b>APLL_CTRL1</b>	<b>7:0</b>	<b>Default : 0xBC</b> <b>Access : R/W</b>
	APL_EN	7	Analog burst-lock PLL Enable.
	APL_TYPE	6:4	APL Type.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	-	3:2	Reserved.
	APL_EN2	1	No state 7, when no bust.
	CLMP_6B_FORCE	0	Clamp value 6-bit test mode enable.
<b>21h</b>	<b>APLL_CTRL2</b>	<b>7:0</b>	<b>Default : 0x18</b> <b>Access : R/W</b>
	CLMP_2DSM	7	Second order Clamp method.
	APL_COMB_LL_TST[1]	6	0: Comb-Line-Lock Disabled if VCR. 1: Com-Line-Lock Enabled even for VCR.
	APL_COMB_LL_TST[0]	5	0: Fractional SYNC Phase is used. 1: Integer PD from Comb.
	DPL_PHS_CAL	4	DPL Phase Calibration.
	APL_CEZANNE	3	For CEZANNE FPGA Test.
	PALSWH_MODE	2:1	PAL Switch Mode control.
	APL_COMB_LL_EN	0	Comb Line-Locked mode Enable.
<b>22h</b>	<b>APL_FREQ_MD</b>	<b>7:0</b>	<b>Default : 0x61</b> <b>Access : R/W</b>
	APL_FREQ_MD[7:5]	7:5	APL Freq Mode.
	-	4:3	Reserved.
	ACLpz_WIDTH	2:0	Clamping Width.
<b>23h</b>	<b>APLL_TRANGE</b>	<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>
	APL_FREQ_LMT	7:5	Burst PLL Frequency Limitation. 0: 125ppm. 2: 250ppm. 4: 500ppm. 6: 1000ppm.
	-	4:1	Reserved.
	APL_K_FORCE	0	APL K value Force enable.
<b>24h</b>	<b>APL_K1_NOISY</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	APL_K1_NOISY[7:0]	7:0	APLL phase tracking coefficients for Noisy broadcast.
<b>25h</b>	<b>APL_K2_NOISY</b>	<b>7:0</b>	<b>Default : 0x02</b> <b>Access : R/W</b>
	APL_K2_NOISY[7:0]	7:0	APLL frequency tracking coefficients for Noisy broadcast.
<b>26h</b>	<b>APL_K1_NORM</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>
	APL_K1	7:0	APLL phase tracking coefficients for normal condition.
<b>27h</b>	<b>APL_K2_NORM</b>	<b>7:0</b>	<b>Default : 0x08</b> <b>Access : R/W</b>
	APL_K2	7:0	APLL frequency tracking coefficients for normal condition.
<b>28h</b>	<b>APL_K1_VCR</b>	<b>7:0</b>	<b>Default : 0x02</b> <b>Access : R/W</b>



### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	APL_K1_VCR	7:0	APLL phase tracking coefficients for VCR.
29h	<b>APL_K2_VCR</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	APL_K2_VCR	7:0	APLL frequency tracking coefficients for VCR.
2Ah	<b>MODE_PFSC</b>	<b>7:0</b>	<b>Default : 0x20</b> <b>Access : R/W</b>
	MD_PFSC[7]	7	0: Auto Fsc. 1: Manual Fsc.
	MD_PFSC[6:4]	6:4	When bit[7]=1, 000: fsc=4.43361875 MHz. 001: fsc=4.406 MHz. 010: fsc=3.579545 MHz. 100: fsc=3.57561149 MHz. 110: fsc=3.58205625 MHz.
	VDFD_ASWFSC	3	Internal blind FSC try.
	VDFD_ASWFSC1	2	Internal blind FSC try1.
	HALFWIN_OP	1	Half Window period Option. 0: Asserted between 1/4 to 3/4 line period. 1: Asserted between 1/2 to 1 line period.
	OEINV_MD	0	ODD_EVEN_INVERT bit inversion Mode. 0: Directly bypass. 1: Inverse.
	2Bh	<b>VDFD_CTRL1</b>	<b>7:0</b>
VDFD_FD_L		7:4	Fast attack frequency tracking time period.
VDFD_PHSSTD_L		3:0	Monitor Phase tracking time period.
2Ch	<b>VDFD_CTRL2</b>	<b>7:0</b>	<b>Default : 0x67</b> <b>Access : R/W</b>
	PHS_DIFF_THRD	7:4	Phase tracking deviation large Threshold.
	PHS_STD_RANGE	3:0	Phase tracking deviation small threshold.
2Dh	<b>FD_K</b>	<b>7:0</b>	<b>Default : 0xC0</b> <b>Access : R/W</b>
	FD_K	7:4	Fast Attack Frequency Tracking Coefficient.
	APL_PHS_OFST[11:8]	3:0	Preferred Phase Offset of the Analog Burst-locked PLL.
2Eh	<b>APL_PHS_OFST</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	APL_PHS_OFST[7:0]	7:0	Preferred Phase Offset of the analog burst-locked PLL.
2Fh	<b>BLACK_SEL</b>	<b>7:0</b>	<b>Default : 0x24</b> <b>Access : R/W</b>

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	SETUP_YES	7:5	0x: Based on confirm mode auto determine. NTSC: setup. PAL: no setup. 10: Force no setup for NTSC. 11: Force setup for PAL.
	-	4:2	Reserved.
	-	1:0	Reserved.
<b>30h</b>	<b>CLAMP_CTRL</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	CLAMPDAC_CTRL[7:6]	7:6	00: Auto clamping control. 01: Auto clamping control, but polarity inverted. 10: Force clamping control by bit[5:0]. 11: Auto clamping control.
	CLAMPDAC_CTRL[5:0]	5:0	Clamping control value.
<b>31h</b>	<b>CLAMP_COEF1</b>	<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>
	CLMP_TYPE_ST3BOT	7	CLMP_BOT function enable in STAE3.
	CLMP_K1	6:0	Clamping speed; the larger the faster. 7'b101_1000 suggested for 1.00 uF. 7'b100_0000 suggested for 0.10 uF. (default) 7'b010_1000 suggested for 0.01 uF.
<b>32h</b>	<b>CLAMP_COEF2</b>	<b>7:0</b>	<b>Default : 0xA0</b> <b>Access : R/W</b>
	CLMP_TYPE	7	Back-porch clamping enable (default =1).
	CLMP_K2	6:0	Leakage current tracking speed. Smaller value is preferred. 7'b001_0000 suggested for 1.00 uF. 7'b010_0000 suggested for 0.10 uF. (default). 7'b011_0000 suggested for 0.01 uF.
<b>33h</b>	<b>CLAMP_COEF3</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CLMP_LKG_MODE	7:4	Leakage control Mode.
	ADCLOSS_CNT	3:0	Count value of ADC Loss status.
<b>34h</b>	<b>CLAMP_COEF4</b>	<b>7:0</b>	<b>Default : 0x82</b> <b>Access : R/W</b>
	CLMP_BOTSPD	7:6	Bottom reference LPF selection.
	CLMP_DLKG_MAC	5:0	Delta leakage is bounded by +- (CLAMP_DLKG_MAX/512).
<b>35h</b>	<b>CLAMP_REF_SEL1</b>	<b>7:0</b>	<b>Default : 0x0A</b> <b>Access : R/W</b>
	BLANKLVL_CTRL	7	Blank Level Control.
	BLANK_LVL[8]	6	Blank Level bit[8].

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	CLMP_LKG	5:0	If CLAMP_LKG_MD = 1011, leakage is forced by CLAMP_LKG[4:0] * sign; where, sign=+1 if bit[5]=1, and sign=-1 if bit[5]=0. Default: 6'd10.
36h	<b>CLAMP_COEF5</b>	<b>7:0</b>	<b>Default : 0x45</b> <span style="float: right;"><b>Access : R/W</b></span>
	CLMP_BOTSEL	7:5	Clamp Bot Selection enable.
	CLMP_ERR_MAX	4:0	Back porch level Error for clamping is bounded by +- CLMP_ERR_MAX*8 (Default: 5'd25).
37h	<b>CLAMP_REF_SEL2</b>	<b>7:0</b>	<b>Default : 0xF0</b> <span style="float: right;"><b>Access : R/W</b></span>
	BLANK_LVL[7:0]	7:0	Blank Level.
38h	<b>VSTROBE_LIMIT</b>	<b>7:0</b>	<b>Default : 0x13</b> <span style="float: right;"><b>Access : R/W</b></span>
	BLACKLVL_CTRL	7	Black Level Control.
	BLACK_LVL[8]	6	Black Level bit[8].
	HV_VCNTSEL	5	1: Enable 2 <sup>nd</sup> Integration Protection for V Extraction.
	HV_VLINPROT	4	0: Enable Next V Extraction after 50 Lines. 1: Enable Next V Extraction after 200 Lines.
	BOTAV_INSEL	3	Bottom of active video Input Selection.
	BOT_INSEL	2:0	Bottom of whole line Input Selection.
39h	<b>VSTROBE_PROTECT</b>	<b>7:0</b>	<b>Default : 0x6C</b> <span style="float: right;"><b>Access : R/W</b></span>
	WP_INSEL	7:5	Sync Input LPF BW Selection.
	HV_INSEL	4:2	HSYNC/VSYNC slicer level Selection.
	TOP_INSEL	1:0	Top level Input Selection.
3Ah	<b>BLACK_LVL</b>	<b>7:0</b>	<b>Default : 0xCC</b> <span style="float: right;"><b>Access : R/W</b></span>
	BLACK_LVL[7:0]	7:0	Black Level value.
3Bh	<b>HV_VEXTH</b>	<b>7:0</b>	<b>Default : 0x7D</b> <span style="float: right;"><b>Access : R/W</b></span>
	HV_VEXTH	7:0	0: V Extract by Line Length Unit. 1: V Extract by Manual Pixel Length Units.
3Ch	<b>HV_C TRL1</b>	<b>7:0</b>	<b>Default : 0x2A</b> <span style="float: right;"><b>Access : R/W</b></span>
	HV_VSEL	7:6	00: V Extract native. 01: V Extrat Native Synchronize to next line start/middle. Other reserved.
	HV_VTHRDSEL	5:4	00: 3/8 line. 01: 6/8 line. 10: 1.25 line. 11: 1.75 line. As Threshold for V Extract.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	HV_INTCNT	3:0	Composite SYNC Pixel Lengths Filter for V Extract.
3Dh	<b>V_POSTCOAST</b>	<b>7:0</b>	<b>Default : 0x00</b>   <b>Access : R/W</b>
	VCOST_FEXT	7:6	Coast forward control.
	VCOST_BEXT	5:0	Coast Backward control.
3Eh	<b>HV_SLICTRL</b>	<b>7:0</b>	<b>Default : 0x0C</b>   <b>Access : R/W</b>
	HV_SLICTRL	7:0	HSYNC/VSYNC Slicer Control.
3Fh	<b>HV_HSLIOFSTHYS</b>	<b>7:0</b>	<b>Default : 0xC0</b>   <b>Access : R/W</b>
	HV_HSLIOFSTHYS	7:4	HSYNC slicer line Offset.
	AGC_FINE_LSB	3:0	AGC Fine gain (lower 4 bits).
40h	<b>PGA_CTRL1</b>	<b>7:0</b>	<b>Default : 0xC1</b>   <b>Access : R/W</b>
	PGA_AUTO	7	0: Manual PGA set by AGC_COARSE[1:0]. 1: Auto PGA switch.
	PGA_FSWT	6	0: PGA switch in VSYNC. 1: PGA switch in HSYNC.
	AGC_COARSE	5:4	00: PGA x 1. 01: PGA x 2.
	FREZ_CLMPDISBK	3	Freeze Clamp Function; VSYNC selection.
	SYNC_MAG_LOW_TH	2:0	If SYNC Magnitude is Low, Freeze HW Clamping 3 times.
41h	<b>PGH_TOP_TH</b>	<b>7:0</b>	<b>Default : 0xDA</b>   <b>Access : R/W</b>
	PGA_TH_TOP	7:0	If AGC_FINE[11:0] >= 16*PGA_TH_TOP[7:0], use smaller PGA and 16*PGA_H2L[7:0].
42h	<b>PGA_BOT_TH</b>	<b>7:0</b>	<b>Default : 0x40</b>   <b>Access : R/W</b>
	PGA_TH_BOT	7:0	If AGC_FINE[11:0] <= 16*PGA_TH_BOT[7:0], use larger PGA and 16*PGA_L2H[7:0].
43h	<b>AGC_CTRL1</b>	<b>7:0</b>	<b>Default : 0x14</b>   <b>Access : R/W</b>
	-	7	Reserved.
	AGC_MD	6:5	00: Auto, REG_AGC_K used for both search and lock. 01: Auto, REG_AGC_K used for search, clipping delta-gain=-1, 0, +1 for lock. 10: Freeze gain. 11: Load gain=AGC_FINE*16. Default=1.
	AGC_LOCK_CTRL	4	AGC Lock Control.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	AGC_TYPE	3:2	00: Sync. 01: Sync. 10: Color burst. 11: Hybrid of 1 and 2. Default=1, HSYNC as primary reference, color burst is for ACC.
	AGC_LOWTH_PGA	1:0	During PGA switching, PGA must be larger than AGC_LOWTH_PGA.
44h	<b>AGC_FINE</b>	<b>7:0</b>	<b>Default : 0xC0</b> <b>Access : R/W</b>
	AGC_FINE	7:0	Used when AGC_MODE=11.
45h	<b>AGC_CTRL2</b>	<b>7:0</b>	<b>Default : 0x42</b> <b>Access : R/W</b>
	AGC_AVGL	7:5	AGC average lines= $2^{AGC\_AVGL + 1}$ .
	-	4	Reserved.
	AGC_WAITL	3:1	Lines to wait for analog settling down= $2^{AGC\_WAITL}$ after each gain update.
	-	0	Reserved.
46h	<b>AGC_K_CTRL</b>	<b>7:0</b>	<b>Default : 0x73</b> <b>Access : R/W</b>
	AGC_K_FAST	7:4	Fast-attack AGC update speed. $\Delta\_gain = \pm (AGC\_K\_FAST * 4 + 3) / 256 * gain\_true$ .
	AGC_K	3:0	Sync magnitude AGC update speed. $\Delta\_gain = amp\_err / 256 * (1 + AGC\_K) / 32 * gan\_true$ .
47h	<b>AGC_CTRL3</b>	<b>7:0</b>	<b>Default : 0x3F</b> <b>Access : R/W</b>
	AGC_BKLCLIP	7:5	AGC Black level Clip enable.
	AGC_CLIP	4:0	The sync magnitude error for AGC is bounded by $\pm 4 * REG\_AGC\_CLIP$ .
48h	<b>PGA_SWTICH_TH1</b>	<b>7:0</b>	<b>Default : 0xC0</b> <b>Access : R/W</b>
	PGA_L2H	7:0	Used when $AGC\_FINE \leq PGA\_TH\_BOT * 16$ . Default: $3072 / 16 = 8'd192$ .
49h	<b>PGA_SWCH_TH2</b>	<b>7:0</b>	<b>Default :</b> <b>Access : R/W</b>
	PGA_H2L	7:0	Used when $AGC\_FINE \leq PGA\_TH\_BOT * 16$ . Default: $1238 / 16 = 8'd64$ .
4Ah	<b>AGC_LOWTH</b>	<b>7:0</b>	<b>Default : 0xA0</b> <b>Access : R/W</b>
	AGC_LOWTH	7:0	When $PGA = AGC\_LOWTH\_PGA$ , $AGC\_FINE[11:0]$ must be smaller than $16 * AGC\_LOWTH$ .
4Bh	<b>PGA_OFST</b>	<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>
	PGA_OFST	7:0	ADC VREF offset = $VREF\_min / (VREF\_max - VREF\_min) * 4096 / 16$ .
4Ch	<b>BRST_WINDOW1</b>	<b>7:0</b>	<b>Default : 0x62</b> <b>Access : R/W</b>

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	BRST_MASK_0	7:5	HSYNC trailing edge transition region Maskout for Burst Calculation.
	BRST_BEG	4:0	Burst window Beginning position; move to SW.
4Dh	<b>BRST_WINDOW2</b>	<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>
	BRST_END	7:0	Burst window End position; move to SW.
4Eh	<b>BK_WINDOW1</b>	<b>7:0</b>	<b>Default : 0x05</b> <b>Access : R/W</b>
	BKPRH_CTR[8]	7	Back-Porch Window Center Position.
	BKPRH_SEL	6	Back-Porch Selection.
	BKPRH_AUTSW	5:4	Back-Porch Auto Switch.
	BKPRH_WIN	3:0	Back-porch Window width=( $*4+4$ ).
4Fh	<b>BK_WINDOW2</b>	<b>7:0</b>	<b>Default : 0x68</b> <b>Access : R/W</b>
	BKPRH_CTR[7:0]	7:0	Back-Porch Window Center Position.
50h	<b>BRST_TH</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	BRST_THRD	7:4	Burst Threshold.
	BRST_AMP_THRD	3:0	Burst found Amplitude Threshold.
51h	<b>BRSTMAG_CTRL</b>	<b>7:0</b>	<b>Default : 0x38</b> <b>Access : R/W</b>
	BRSTMAG_CTRL	7	Burst Magnitude Control.
	BRST_MAG[8:2]	6:0	Burst Magnitude value.
52h	<b>COMB_LL_CTRL</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	BRST_MAG[1:0]	7:6	Burst Magnitude value.
	-	5:4	Reserved.
	PAL_BLIND_PD_EN	3	NTSC; 180 degree Phase Detection Enable.
	BRST_PHS_CHK_MAG	2	Burst Phase of the current line is ignored if $BRST\_MAG < BRST\_MAG\_AVG/8$ .
	-	1:0	Reserved.
53h	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
54h	<b>BRST_WINDOW3</b>	<b>7:0</b>	<b>Default : 0x23</b> <b>Access : R/W</b>
	FSC_THRD_LINES	7:5	FSC Threshold Lines.
	-	4:3	Reserved.
	FSC_TST_TRY[2]	2	Fsc selection 1.25*Fsc and 0.8*Fsc BPF magnitude type.
	FSC_TST_TRY[1]	1	Fsc selection 1.0*Fsc BPF magnitude type.
	FSC_TST_TRY[0]	0	Fsc selection BPF magnitude snapshot taken at the end of the burst window.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	Access
55h	<b>COLOR_OFF</b>	<b>7:0</b>	<b>Default : 0x08</b>	<b>Access : R/W</b>
	KILL_CSPOUT	7:6	00 or 01: Auto Color Kill. 10: Force Show Color. 11: Force Kill Color.	
	-	5	Reserved.	
	PAL_LINES_TH	4:0	Lines for PAL/NTSC detection=64 * PAL_LINES_TH.	
56h	<b>FSC443/357 DECT1</b>	<b>7:0</b>	<b>Default : 0x18</b>	<b>Access : R/W</b>
	-	7:6	Reserved.	
	FSC_THRD1_PASS	5:0	FSC Threshold1 Pass.	
57h	<b>FSC443/357 DECT2</b>	<b>7:0</b>	<b>Default : 0x28</b>	<b>Access : R/W</b>
	-	7:6	Reserved.	
	FSC_THRD1_FAIL	5:0	FSC Threshold1 Fail.	
58h	<b>FSC443/357 DECT3</b>	<b>7:0</b>	<b>Default : 0x10</b>	<b>Access : R/W</b>
	-	7:6	Reserved.	
	FSC_THRD0_PASS	5:0	FSC Threshold0 Pass.	
59h	<b>FSC443/357 DECT4</b>	<b>7:0</b>	<b>Default : 0x20</b>	<b>Access : R/W</b>
	-	7:6	Reserved.	
	FSC_THRD0_FAIL	5:0	FSC Threshold0 Fail.	
5Ah	<b>BRST_UNKNOW_TH</b>	<b>7:0</b>	<b>Default : 0x10</b>	<b>Access : R/W</b>
	-	7	Reserved.	
	FSC_TST_MASK	6:4	HSYNC trailing edge Transition region Maskout for Fsc selection filters.	
	FSC_THRD_NO_BRST	3:0	FSC Threshold for No Burst detection.	
5Bh	<b>FSC443/357 DECT5</b>	<b>7:0</b>	<b>Default : 0x98</b>	<b>Access : R/W</b>
	FSC_THRD_MAG_HYST[3:2]	7:6	FSC Threshold Magnitude of HSYNC start.	
	FSC_THRD_MAG_443	5:0	FSC Threshold Magnitude of 4.43 MHz.	
5Ch	<b>FSC443/357 DECT6</b>	<b>7:0</b>	<b>Default : 0x98</b>	<b>Access : R/W</b>
	FSC_THRD_MAG_HYST[1:0]	7:6	FSC Threshold Magnitude of HSYNC start.	
	FSC_THRD_MAG_358	5:0	FSC Threshold Magnitude of 3.58 MHz.	
5Dh	<b>ACC_CTRL</b>	<b>7:0</b>	<b>Default : 0x08</b>	<b>Access : R/W</b>

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	ACC_CTRL	7:6	Auto Chroma Control. 01: Reset Chroma_Gain=1. 11: Load Chroma_Gain=ACC_GAIN[13:0]/64.
	ACC_GAIN[5:0]	5:0	Auto-Chroma-Control Gain.
<b>5Eh</b>	<b>ACC_GAIN</b>	<b>7:0</b>	<b>Default : 0x20</b> <b>Access : R/W</b>
	ACC_GAIN[13:6]	7:0	Auto-Chroma-Control Gain.
<b>5Fh</b>	<b>AGC_DELTA</b>	<b>7:0</b>	<b>Default : 0x28</b> <b>Access : R/W</b>
	AGC_DELTA[7:5]	7:5	AGC Delta value.
	WP_SIM_SPD	4:3	WP Simulation Speedup.
	WP_LVL_SPD	2:0	WP Level Speedup.
<b>60h</b>	<b>WP_CTRL1</b>	<b>7:0</b>	<b>Default : 0x15</b> <b>Access : R/W</b>
	ACC_C_PEAK_LPF	7:6	Chroma Peak Detection Update Speed. 00: Slow, Narrow-Band-Width. 11: Fast, Wide-Band-Width.
	-	5	Reserved.
	WP_TH[8]	4	Desired white level=512+REG_WP_TH.
	AGC_K_WP	3:0	White peaking AGC update speed. Delta_gain=white_err/256*(1+REG_AGC_K)/ 32*gain_true.
<b>61h</b>	<b>WP_THRD</b>	<b>7:0</b>	<b>Default : 0x24</b> <b>Access : R/W</b>
	WP_THRD[7:0]	7:0	White Peak Threshold value.
<b>62h</b>	<b>AP_SYNTHRD2REAGC</b>	<b>7:0</b>	<b>Default : 0x78</b> <b>Access : R/W</b>
	WP_SYNTHRD2REAGC	7:0	WP Sync Threshold of AGC.
<b>63h ~</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
<b>64h</b>	-	7:0	Reserved.
<b>65h</b>	<b>AGC_CTRL4</b>	<b>7:0</b>	<b>Default : 0x55</b> <b>Access : R/W</b>
	-	7:2	Reserved.
	WP_WAITTH	1:0	Number of sync-mag AGC operations before WP mode. 00: 255 operations. 01: 127 operations. 10: 63 operations. 11: 31 operations.
<b>66h</b>	<b>WP_CTRL2</b>	<b>7:0</b>	<b>Default : 0x70</b> <b>Access : R/W</b>



### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	WP_MODE	7:5	0xx: Internally automatic white-peaking control. 100: Disable white-peaking. 101: Hold sync magnitude AGC if white level is too high. 110: Reserved. 111: Normal white-peaking AGC.
	WP_MONTR_SPD	4:2	WP Monitor Speed.
	ADCOVSLE_THRD	1:0	WP Threshold Selection.
<b>67h</b>	<b>WP_REDO</b>	<b>7:0</b>	<b>Default : 0x17</b> <b>Access : R/W</b>
	ROUND_CTRL	7:5	AFEC signal rounding selection.
	REMOV_HF_NOISE	4	Enable 13-tap CVBS low-pass filter to Remove High-Frequency Noise.
	ROUND_CTRL[3:2]	3:2	7-tap chroma-trap filter, CCTRAP, Rounding. 00: Truncate. 01: Round. 10: Dither.
	ROUND_CTRL[1]	1	AFEC self-test 1D luminance Rounding. 0: Truncate. 1: Round.
	ROUND_CTRL[0]	0	AFEC self-test 1D chroma Rounding. 0: Truncate. 1: Round.
<b>68h</b>	<b>CLK_CTRL1</b>	<b>7:0</b>	<b>Default : 0x45</b> <b>Access : R/W</b>
	ADC_84_ROUND	7:6	Round control for 8Fsc-to-4Fsc downsampling. 0: Truncate. 1: Round.
	DAC_LATCH_INV	5	Option for Datalatch from 4Fsc to 8Fsc.
	3DAC_EN	4	Enable AFEC Data Output to DAC.
	FILSEL	3:2	Filter Selection.
	ADC_168_ROUND	1:0	Round Control for 16Fsc-to-8Fsc Downsampling. 0: Truncate. 1: Round.
<b>69h</b>	<b>SRC_CTRL1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	SELYC	7	0: YC Source from AFEC for Testing Purpose. 1: YC Source from Comb for Display.
	-	6:5	Reserved.
	BYPASS_Y	4	Bypass CVBS Source for Testing purpose.
	COMB601H_SYNC	3	1: Use the HS444 as the MVDA_HS Output.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	COMB601V_SYNC	2	1: Use the VS444 as the MVDA_VS Output.
	COMB601F_SYNC	1	1: Use the Fld444 as the MVDA_F Output.
	COMBPASS_SYNC	0	1: The HS444 and VS444 as the Bypass SYNC. 0: AFEC_HS and AFEC_VS as the Bypass SYNC Output.
<b>6Ah</b>	<b>VCR_DETECT1</b>	<b>7:0</b>	<b>Default : 0x51</b> <b>Access : R/W</b>
	VCR_MODE	7:6	VCR Mode enable.
	VCR_HD_DLY	5:4	VCR Head switch number.
	-	3	Reserved.
	VS_STB	2:0	VS Strobe.
<b>6Bh</b>	<b>VCR_DETECT2</b>	<b>7:0</b>	<b>Default : 0xAA</b> <b>Access : R/W</b>
	VCR_LDT	7:4	VCR Line Margin.
	FAST_VT_DET	3	Fast Vertical Line Detection.
	VCR_THRD	2:0	VCR Threshold.
<b>6Ch</b>	<b>VCR_PRECOAST</b>	<b>7:0</b>	<b>Default : 0xF0</b> <b>Access : R/W</b>
	VCR_PRECOAST	7:4	Pre-Coast value for VCR mode.
	HV_HSLISEL_VCR	3:2	HSYNC Slicer Selection for VCR mode.
	HV_SLILOW_SEL	1:0	HSYNC/VSYSNCR slicer Low Selection.
<b>6Dh</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
<b>6Eh</b>	<b>VCR_VLSET</b>	<b>7:0</b>	<b>Default : 0x14</b> <b>Access : R/W</b>
	VCR_VLSET	7:0	PAC/NTSC VLine tuning.
<b>6Fh</b>		<b>7:0</b>	<b>Default :</b> <b>Access :</b>
	RST_AFEC_SEL	7	0: Partial reset AFEC. 1: Global reset AFEC.
	-	6:4	Reserved.
	DPL_DDE_EN	3	DPL double DE Enable.
	DDE_EN	2	Double DE Enable.
	DPL_HS_EN	1	DPL HS Enable.
	DPL_DE_EN	0	DPL DE Enable.
<b>70h</b>	<b>INI_CTRL1</b>	<b>7:0</b>	<b>Default : 0x84</b> <b>Access : R/W</b>
	FSTAGC_EN	7	Fast AGC mode.
	-	6	Reserved.
	CLMP_BOTMD	5:4	Clamp on Bottom Mode.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	ADSMAL_THRD	3:0	Threshold for detecting Small AOC swing.
71h	<b>BOTREF_LVL</b>	<b>7:0</b>	<b>Default : 0xA0</b> <b>Access : R/W</b>
	BOTREF_LVL	7:0	Bottom Reference Level.
72h	<b>HV_SLC_CTRL</b>	<b>7:0</b>	<b>Default : 0x37</b> <b>Access : R/W</b>
	HV_SLCFZE	7:6	HSYNC/VSYNC Slice Freeze control.
	HV_SLCDIF	5:4	HSYNC/VSYNC Slice Difference.
	HV_SLCDLT	3:0	HSYNC/VSYNC Slice Limit.
73h	<b>INI_CTRL1</b>	<b>7:0</b>	<b>Default : 0x52</b> <b>Access : R/W</b>
	HV_VSLISEL	7:6	00: 2/8 syn_magnitude as hslice level. 01: 4/8 syn_magnitude as hslice level. 10: 5/8 syn_magnitude as hslice level. 11: 6/8 syn_magnitude as hslice level.
	HV_HSLISEL	5:4	00: 2/8 syn_magnitude as vslice level. 01: 4/8 syn_magnitude as vslice level. 10: 5/8 syn_magnitude as vslice level. 11: 6/8 syn_magnitude as vslice level.
	656_HDES_VCR_OFST	3:0	656 SAV Position Offset when VCR.
74h	<b>SLICE_MUX</b>	<b>7:0</b>	<b>Default : 0x97</b> <b>Access : R/W</b>
	SLICE_MUX	7:0	Slicer level selection.
75h	<b>656_OFST</b>	<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>
	-	7	Reserved.
	656_OFST	6:0	56 SAV Position Offset in VCR mode.
76h	<b>656_CTRL1</b>	<b>7:0</b>	<b>Default : 0x02</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	DBCLK_TEST	4	Clock Testing.
	-	3	Reserved.
	656_BLNK_MD	2	656 Blank Mode.
	656_EN	1	Enable 656 mode.
	ABNML_CHK	0	Abnormal check enable.
77h	<b>656_BLNK_MAX</b>	<b>7:0</b>	<b>Default : 0x02</b> <b>Access : R/W</b>
	656_BLNK_MAX[7:0]	7:0	656 Blink Max value.
78h	<b>YUV</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	YUV[7:0]	7:0	Used as Input of the 4Fsc-to-16Fsc Up-sampling if SELUPS=3.
79h	<b>656_HDES1</b>	<b>7:0</b>	<b>Default : 0x18</b> <b>Access : R/W</b>

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	656_HDES_O[9:2]	7:0	SDA start position. (656_HDESM, 656_HDESL) ITU656 SAV Position. For VCR, 656_HDES=656_HDES_o-656_HDES_VCR_OFST*4. Otherwise, 656_HDES=656_HDES_o.
<b>7Ah</b>	<b>656_HDES2</b>	<b>7:0</b>	<b>Default : 0x20</b> <b>Access : R/W</b>
	656_HDES_O[1:0]	7:6	ITU656 SAV position.
	-	5:2	Reserved.
	656_INV_F	1	656 Field Inverse.
	-	0	Reserved.
<b>7Bh</b>	<b>656_HDEW</b>	<b>7:0</b>	<b>Default : 0xB3</b> <b>Access : R/W</b>
	656_HDEW	7:0	ITU656 active data Width (*8+7).
<b>7Ch</b>	<b>SLMIS_CTRL</b>	<b>7:0</b>	<b>Default : 0xC0</b> <b>Access : R/W</b>
	SLMIS_CTRL[7:0]	7:0	Enable Slice Miss freeze.
<b>7Dh</b>	<b>NOISE_MLINE</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	NOISE_MLINE	7:0	Move Noise level during specify Line Number.
<b>7Eh</b>	<b>656_CTRL2</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	656_CLKINV	7	Used for FPGA testing.
	656_CLKDLY	6:5	Used for FPGA testing.
	656_LSTSEL	4	Used for FPGA testing.
	656_TEST	3:2	Used for FPGA testing.
	TEST_MODE	1:0	Used for FPGA testing.
<b>7Fh</b>	<b>444_VD_CTRL</b>	<b>7:0</b>	<b>Default : 0x62</b> <b>Access : R/W</b>
	SELDAC	7:6	Source for 3 DACs. 00: Comb. 01: AFEC Test Mode. 10: 444. 11: Upsampling Source.
	3DAC_INSHV	5	Insert HV into Display DAC Source.
	3DAC_HSEL	4	Insert H's Source Selection. 0: Window PLL. 1: Display PLL.
	3DAC_INSBLACK	3	Insert Black Level back to DAC Source.
	REG_SELFB	2	0: YCbCr Source from AFEC Test Mode. 1: YCbCr Source from Comb444.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	REG_SELUPS	1:0	Upsampling Source. 10: Test Mode 444. 11: Comb YCbCr 444.
80h	<b>NCO_FSC0</b>	<b>7:0</b>	<b>Default : 0x48</b> <b>Access : R/W</b>
	FSC_NCO0[23:16]	7:0	{NCO_FSC0} 4.43 MHz synthesis clock. Frequency Synthesizer 4*Fsc for 4.43361875 MHz. (For REG_FSC_TABLE[4]=0.) Synthesis-base/(4*Fsc)*2 <sup>22</sup> /8.
81h	<b>NCO_FSC0</b>	<b>7:0</b>	<b>Default : 0x2D</b> <b>Access : R/W</b>
	FSC_NCO0[15:8]	7:0	{NCO_FSC0} 4.43 MHz synthesis clock.
82h	<b>NCO_FSC0</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	FSC_NCO0[7:0]	7:0	{NCO_FSC0} 4.43 MHz synthesis clock.
83h	<b>NCO_FSC1</b>	<b>7:0</b>	<b>Default : 0x59</b> <b>Access : R/W</b>
	FSC_NCO1[23:16]	7:0	Frequency synthesizer 4*Fsc for 3.57954545 MHz (For FSC_TABLE[4]=0).
84h	<b>NCO_FSC1</b>	<b>7:0</b>	<b>Default : 0x65</b> <b>Access : R/W</b>
	FSC_NCO1[15:8]	7:0	{NCO_FSC1} 3.579 MHz synthesis clock.
85h	<b>NCO_FSC1</b>	<b>7:0</b>	<b>Default : 0x97</b> <b>Access : R/W</b>
	FSC_NCO1[7:0]	7:0	{NCO_FSC1} 3.579 MHz synthesis clock.
86h	<b>NCO_FSC2</b>	<b>7:0</b>	<b>Default : 0x59</b> <b>Access : R/W</b>
	FSC_NCO2[23:16]	7:0	Frequency Synthesizer 4*Fsc for 3.57561149 MHz (For FSC_TABLE[4] = 0).
87h	<b>NCO_FSC2</b>	<b>7:0</b>	<b>Default : 0x7E</b> <b>Access : R/W</b>
	FSC_NCO2[15:8]	7:0	{NCO_FSC2} 3.582 MHz synthesis clock.
88h	<b>NCO_FSC2</b>	<b>7:0</b>	<b>Default : 0x74</b> <b>Access : R/W</b>
	FSC_NCO2[7:0]	7:0	{NCO_FSC2} 3.582 MHz synthesis clock.
89h	<b>NCO_FSC3</b>	<b>7:0</b>	<b>Default : 0x59</b> <b>Access : R/W</b>
	FSC_NCO3[23:16]	7:0	Frequency Sunthesizer 4*Fsc for 3.58205625 MHz (For FSC_TABLE[4] = 0).
8Ah	<b>NCO_FSC3</b>	<b>7:0</b>	<b>Default : 0x55</b> <b>Access : R/W</b>
	FSC_NCO3[15:8]	7:0	{NCO_FSC3} 3.576 MHz synthesis clock.
8Bh	<b>NCO_FSC3</b>	<b>7:0</b>	<b>Default : 0x8B</b> <b>Access : R/W</b>
	FSC_NCO3[7:0]	7:0	{NCO_FSC3} 3.576 MHz synthesis clock.
8Ch	<b>REG_FSC_NCO4</b>	<b>7:0</b>	<b>Default : 0x4A</b> <b>Access : R/W</b>

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	FSC_NCO4[23:16]	7:0	Requency Synthesizer 4*Fsc for 4.28515625 MHz (For REG_FSC_TABLE[4] = 0).
8Dh	<b>FSC_NCO4</b>	<b>7:0</b>	<b>Default : 0xAD</b> <b>Access : R/W</b>
	FSC_NCO4[15:8]	7:0	Requency Synthesizer 4*Fsc for 4.28515625 MHz (For REG_FSC_TABLE[4] = 0).
8Eh	<b>FSC_NCO4</b>	<b>7:0</b>	<b>Default : 0x27</b> <b>Access : R/W</b>
	FSC_NCO4[7:0]	7:0	Requency Synthesizer 4*Fsc for 4.28515625 MHz (For REG_FSC_TABLE[4] = 0).
8Fh	<b>FSC_TABLE</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:5	Reserved.
	FSC_TABLE[4]	4	Frequency Synthesizer Control. 0: FSC_NCO0, 1, 2, 3, and 4 are used. 1: Specified by FSC_TABLE[3:2].
	FSC_TABLE[3:2]	3:2	Frequency Synthesizer Base. 00: 160MHz. 01: 15*14.31818MHz. 10: 216MHz. 11: 15*14.31818MHz. Only valid for FSC_TABLE[4] =1.
	FSC_TABLE[1:0]	1:0	Frequency Synthesizer Output. 00: 4*FSC. 01: 8*FSC. 10: 16*FSC. 11: 16*FSC.
90h	<b>FSC_NCO_ERR_443</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	FSC_NCO_ERR_443 [15:8]	7:0	Frequency Synthesizer 4*Fsc Error for 4.43MHz; 2's Complement (Auto scaled internally for 3.58MHz).
91h	<b>FSC_NCO_ERR_443</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	FSC_NCO_ERR_443 [7:0]	7:0	Frequency Synthesizer 4*Fsc Error for 4.43MHz; 2's Complement (Auto scaled internally for 3.58MHz).
92h	<b>WINIIR_THRD_CTRL</b>	<b>7:0</b>	<b>Default : 0xA7</b> <b>Access : R/W</b>
	WINIIR_THRD1	7:4	IIR Window Threshold 1.
	WINIIR_THRD0	3:0	IIR Window Threshold 0.
93h	<b>WINFIR_THRD_CTRL</b>	<b>7:0</b>	<b>Default : 0xA4</b> <b>Access : R/W</b>
	WINFIR_THRD1	7:4	IIR Window Threshold 1.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	WINFIR_THRD0	3:0	IIR Window Threshold 0.
94h	<b>SPL_SPD_CTRL1</b>	<b>7:0</b>	<b>Default : 0x14</b> <b>Access : R/W</b>
	SPL_SPD_FORCE	7:5	Coarse HSYNC PLL Tracking Speed. Bit[2] forces using Bit[1:0]. SPL_SPD=3: Fastest. SPL_SPD=0: Slowest.
	SPL_SPD_SRCH	4:3	Coarse HSYNC PLL tracking Speed during HSYNC-Search.
	SPL_SPD_CLEAN	2:1	Coarse HSYNC PLL tracking Speed for Clean signal.
	-	0	Reserved.
95h	<b>SPL_SPD_CTRL2</b>	<b>7:0</b>	<b>Default : 0x2A</b> <b>Access : R/W</b>
	SPL_SPD_NOISY	7:6	Coarse HSYNC PLL tracking Speed for Noisy signal.
	SPL_SPD_VCR	5:4	Coarse HSYNC PLL phase tracking Speed for VCR outside VSYNC.
	SPL_SPD_VCR_V	3:2	Coarse HSYNC PLL Phase Tracking Speed for VCR during VSYNC.
	SPL_SPD_VCR_PRE	1:0	Coarse HSYNC PLL HSYNC-search lines. 00: 48. 01: 64. 10: 80. 11: 96.
96h	<b>EDGES_NOISY_THR D</b>	<b>7:0</b>	<b>Default : 0xA0</b> <b>Access : R/W</b>
	NOISE_DC_SEL	7:6	Noise magnitude estimation DC level Selection. 00: IIR_8. 01: IIR_8. 10: CCTRAP_13. 11: CCTRAP.
	EDGES_NOISY	5:0	Threshold of the average number of sliced Edges per Line to determine Noisy mode (/ 4).
97h	<b>EDGES_CLEAN_THR D</b>	<b>7:0</b>	<b>Default : 0x05</b> <b>Access : R/W</b>
	SYNC_INMUX[2:1]	7:6	Slicer input pre-filter selection. 00: CCTRAP. 01: CCTRAP_13. 10: IIR_8. 11: IIR_16.
	SYNC_INMUX[0]	5	Slicer Auxiliary Pre-Filter Selection. 0: IIR_8. 1: IIR_16.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	-	4	Reserved.
	EDGES_CLEAN	3:0	Threshold of the average number of sliced Edges per line to determine Clean mode (/ 4).
<b>98h</b>	<b>SYNC_WIN_CTRL1</b>	<b>7:0</b>	<b>Default : 0x43</b> <b>Access : R/W</b>
	SYNC_INMUX_VCR [2:0]	7:5	HSYNC slicer Input selection.
	-	4	Reserved.
	WIN_NOISY	3:0	Coarse HSYNC PLL PD Limitation Window Width for Noisy Mode (*8+7).
<b>99h</b>	<b>SYNC_WIN_CTRL2</b>	<b>7:0</b>	<b>Default : 0x88</b> <b>Access : R/W</b>
	SYNC_WIN	7:4	Coarse HSYNC PLL SYNC-lost detection Window width (*4+4).
	SYNC_WIN_SRCH	3:0	Coarse HSYNC PLL SYNC-found detection Window width (*4+4).
<b>9Ah</b>	<b>SYNC_CTRL1</b>	<b>7:0</b>	<b>Default : 0xF0</b> <b>Access : R/W</b>
	SYNC_THRD_MISS	7:4	Coarse HSYNC PLL SYNC search fail Threshold.
	-	3:2	Reserved.
	SPL_SRCH LENG	1:0	SPL Search Length.
<b>9Bh</b>	<b>SYNC_CTRL2</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	SYNC_THRD	5:0	Coarse HSYNC PLL SYNC search pass (SYNC Found) Threshold (*4+3).
<b>9Ch</b>	<b>SYNC_CTRL3</b>	<b>7:0</b>	<b>Default : 0x1C</b> <b>Access : R/W</b>
	-	7	Reserved.
	SYNC_THRD_LOST	6:0	Coarse HSYNC PLL SYNC SYNC-Lost Threshold (*16+15).
<b>9Dh</b>	<b>DPL_NSPL_HIGH</b>	<b>7:0</b>	<b>Default : 0x6C</b> <b>Access : R/W</b>
	DPL_NSPL[10:3]	7:0	PI-Type Display PLL Number of Samples per Line (MSB); typically 864.
<b>9Eh</b>	<b>DPL_NSPL_LOW</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	DPL_NSPL[2:0]	7:5	PI-type Display PLL Number of Samples per Line (LSB); typically 864.
	DPLL_TRUE8FSC	4	DPLL under 8 Fsc mode.
	-	3:0	Reserved.



### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
9Fh	<b>SPL_K2_VCR</b>	<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>
	SPL_K2_VCR	7:6	Coarse HSYNC PLL Frequency Tracking Speed for VCR.
	SPL_NSPL_LMT	5:0	PI-type display PLL frequency coasts if the coarse HSYNC PLL deviation is larger than +/- 4*SPL_NSPL_LMT (Try).
A0h	<b>DPL_K1_FORCE</b>	<b>7:0</b>	<b>Default : 0x20</b> <b>Access : R/W</b>
	DPL_K_FORCE	7	Force DPL K value.
	-	6	Reserved.
	DPL_K1	5:0	PI-type Display PLL phase tracking coefficient K1.
A1h	<b>DPL_K2_FORCE</b>	<b>7:0</b>	<b>Default : 0x60</b> <b>Access : R/W</b>
	DPL_K2	7:0	PI-type Display PLL frequency tracking coefficient K2.
A2h	<b>DPL_K1_NOISY</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	DPL_K1_NOISY	5:0	PI-type Display PLL phase tracking coefficient for Noisy broadcast.
A3h	<b>DPL_K2_NOISY</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	DPL_K2_NOISY	7:0	PI-type Display PLL frequency tracking coefficient for Noisy broadcast.
A4h	<b>DPL_K1_VCR</b>	<b>7:0</b>	<b>Default : 0x34</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	DPL_K1_VCR	5:0	PI-type Display PLL phase tracking coefficient for VCR.
A5h	<b>DPL_K2_VCR</b>	<b>7:0</b>	<b>Default : 0x6A</b> <b>Access : R/W</b>
	DPL_K2_VCR	7:0	PI-type Display PLL frequency tracking coefficient for VCR.
A6h	<b>DPL_K1_VCR_V</b>	<b>7:0</b>	<b>Default : 0x34</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	DPL_K1_VCR_V	5:0	PI-type Display PLL phase tracking coefficient for VCR during VSYNC.
A7h	<b>DPL_K2_VCR</b>	<b>7:0</b>	<b>Default : 0x2C</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	DPL_VCR_FADE_SPD	5:4	PI-type Display PLL PD_MAX fading speed from VSYNC to active lines. 00: Slow. 11: Fast.
	DPL_VCR_FADE_START	3:0	PI-type Display PLL PE_MAX fading Start lines (*2).
A8h	<b>DPL_K1_FAST</b>	<b>7:0</b>	<b>Default : 0x30</b> <b>Access : R/W</b>
	-	7:6	Reserved.

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	DPL_K1_FAST	5:0	PI-type Display PLL phase tracking coefficient for Fast mode and initialization.
A9h	<b>DPL_K2_FAST</b>	<b>7:0</b>	<b>Default : 0x65</b> <b>Access : R/W</b>
	DPL_K2_FAST	7:0	PI-type Display PLL frequency tracking coefficient for Fast mode and initialization.
AAh	<b>DPL_CTRL1</b>	<b>7:0</b>	<b>Default : 0x08</b> <b>Access : R/W</b>
	-	7:4	Reserved.
	DPL_FAST_LINES	3:0	PI-type Display PLL Fast Mode Lines. (*256)
ABh	<b>DPL_PD_MAX</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>
	DPL_PD_MAX	7:0	PI-type Display PLL Phase Detector (DPL_PD) Limit. If bit[7]=1, force using bit[6:0].
ACh	<b>DPL_PD_MAX_VCR</b>	<b>7:0</b>	<b>Default : 0xFF</b> <b>Access : R/W</b>
	DPL_PD_MAX_VCR	7:0	PI-type Display PLL phase detector (DPL_PD) limit for VCR outside VSYNC area.
ADh	<b>REG_656_CTRL</b>	<b>7:0</b>	<b>Default : 0x3A</b> <b>Access : R/W</b>
	REG_656_OPTION1	7	Line Middle Method 0 Selection.
	REG_656_OPTION0	6	Line Middle Method 1 Selection.
	REG_DPL_WAIT_LENG	5:4	DPL Wait Length.
	REG_DPL_NCO_RST	3	DPL NCO Reset enable.
	DPL_FAST_RE_DO	2	PI-type Display PLL Re-Do Fast Mode.
	DPL_NO_STOP	1	PI-type Display PLL Never Stops. (Free Run when HSYNC not found.)
	DPL_COAST_T_FORCE	0	PI-type Display PLL Frequency Frozen Always. (except when Fast Mode and Initialization)
AEh	<b>DPL_COAST_CTRL</b>	<b>7:0</b>	<b>Default : 0xB8</b> <b>Access : R/W</b>
	VSYNC_SEL	7	VSYNC source Selection.
	-	6	Reserved.
	COAST_V_ALWAYS	5	Always V Coast function.
	DPL_COAST_T_LINES	4:0	Lines where 656 PLL coast frequency during V. PI-type Display PLL Frequency Frozen Lines during VSYNC. (*2)
AFh	<b>DPL_CTRL2</b>	<b>7:0</b>	<b>Default : 0x85</b> <b>Access : R/W</b>
	DPL_LOST_LINES	7:4	PI-type Display PLL Threshold on Lines to Determine Out-of-Lock. (*64).
	DPL_LOST_WIN	3:0	PI-type Display PLL HSYNC Window Width to Detect Out-of-Lock. (*8)

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	Access
<b>B0h</b>	<b>DPL_K1_FREE</b>	<b>7:0</b>	<b>Default : 0x86</b>	<b>Access : R/W</b>
	DPL_K1_FREE	7:4	PI-type Display PLL Phase Tracking Coefficient during HSYNC not found.	
	BKPRH_JUMP_MAX	3:0	Back-Porch-Jump Maximal Lines. (Try.) (Can move to SW Clmp.)	
<b>B1h</b>	<b>BKPRH_JUMP_CTRL</b>	<b>7:0</b>	<b>Default : 0x06</b>	<b>Access : R/W</b>
	-	7	Reserved.	
	BKPRH_JUMP_MV_EN	6:5	Back-Porch-Jump used to Pause Clamping when Macrovision found (if set 01). (Try.) (Can move to SW Clmp.)	
	BKPRH_JUMP_THRD	4:0	Back-Porch-Jump Threshold. (*32+32). (Try.) (Can move to SW Clmp.)	
<b>B2h</b>	<b>SPL_DELAY_FIR</b>	<b>7:0</b>	<b>Default : 0x19</b>	<b>Access : R/W</b>
	-	7:6	Reserved.	
	SPL_DELAY_FIR	5:0	Coarse HSYNC PLL Delay with Respect to the Actual HSYNC Leading Edge if SYNC_INMUX selects CCTRAP or CCTRAP_13.	
<b>B3h</b>	<b>SPL_DELAY_IIR</b>	<b>7:0</b>	<b>Default : 0x1E</b>	<b>Access : R/W</b>
	-	7	Reserved.	
	SPL_DELAY_IIR	6:0	Coarse HSYNC PLL Delay with Respect to the Actual HSYNC Leading Edge if SYNC_INMUX selects IIR_8 or IIR_16.	
<b>B4h</b>	<b>REG_PB_CTRL</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	REG_PB_EN	7	0: Hold ADC Data Probe. 1: Enable ADC Data Probe.	
	REG_PB_4FSC	6	0: Probe 8Fsc ADC Data when 8Fsc Clock. 1: Probe 4Fsc ADC Data when 8Fsc Clock.	
	REG_PB_LINE	5:4	1: Probe ADC Data in Next Line.	
	REG_PB_YC	3	0: Probe Y(CBVS) ADC Data. 1: Probe C ADC Data.	
	REG_PB_10B	2	0: Probe 8 bit Data. 1: Probe 10 bit Data.	
	-	1:0	Reserved.	
<b>B5h</b>	<b>PROBE_OUT</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R</b>
	PROBE_OUT	7:0	ADC Probe Data. (RP_LSB) ? {6'b0, PROBE_OUT1[1:0]} : PROBE_OUT1[9:2].	
<b>B6h</b>	<b>REG_PB_HPOS</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>

### Video Decoder Register (Bank = 02)

Index	Name	Bits	Description
	REG_PB_HPOS[7:0]	7:0	Start Probe Horizontal Position. (lower 8 bits)
<b>B7h</b>	<b>REG_PB_BPOS1</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:6	Reserved.
	REG_PB_VPOS[10:8]	5:4	Start Probe Vertical Position. (upper 3 bits)
	REG_PB_HPOS[10:8]	2:0	Start Probe Horizontal Position. (upper 3 bits)
<b>B8h</b>	<b>REG_PB_VPOS2</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	REG_PB_VPOS[7:0]	7:0	Start Probe Vertical Position. (lower 8 bits)
<b>B9h</b>	<b>REG_WP_HOVER THRD</b>	<b>7:0</b>	<b>Default : 0x1F</b> <b>Access : R/W</b>
	REG_WP_HOVER THRD[7:0]	7:0	Overflow Threshold of ADC Value.
<b>BAh</b>	<b>REG_WP_HUNDERT HRD</b>	<b>7:0</b>	<b>Default : 0x1F</b> <b>Access : R/W</b>
	REG_WP_HUNDER THRD[7:0]	7:0	Underflow Threshold of ADC Value.
<b>BBh ~ FFh</b>	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.

### Comb-Filter Register (Bank = 03, Registers 01h ~ 9Fh)

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)			
Index	Name	Bits	Description
<b>00h ~ 09h</b>	-	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:0	Reserved.
<b>10h</b>	<b>COMBCFGA</b>	<b>7:0</b>	<b>Default : 0x12</b> <b>Access : R/W</b>
	-	7	Reserved.
	SVDOCBP	6	Band Pass Filter for S-Video C Channel to kill the DC Level.
	DIRADCIN	5	Direct use ADC Input (Bypass AFEC).
	DDETSRCSEL	4	Degree Detect Source Select. 0: Without ACC. 1: After ACC.
	MANUCOMB	3	0: Auto Select Working Mode. 1: Manual Select Working Mode.

**Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	WORKMD	2:0	Working Mode. 000: Off. 001: Notch. 010: 2D Comb. 011: 3D Comb. 100: 3D Comb with History.
<b>11h</b>	<b>COMBCFGB</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	FORCE8BIT	7	Force 8 bit.
	GOODHS	6	Using Free Run HSYNC in Standard Input.
	AFEC_DEM	5	Select AFEC Demodulation.
	PALCMINV	4	PalCmpUp Inverse.
	-	3	Reserved.
	SYNCONY	2	SYNC on Y.
	CRMA_OFF	1	Turn Off the Chroma of video decoder output. 0: Normal. 1: Off.
	BST_OFF	0	Turn Off the Color Burst of video decoder output. 0: Normal. 1: Off.
<b>12h</b>	<b>COMBCFGC</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>
	FREESYNC	7	H/V SYNC Free Run.
	FREECNTMD	6	Free Run Counter Mode. 0: NTSC. 1: PAL.
	SNOWTYPE	5:4	Snow Type. 00: Never snow. 01: Snow when VDOMD = 7. 10, 11: Force snow.
	RND_MD	3:2	Rounding Mode. 00: Truncate. 01: Rounding. 10: Dithering. 11: Error Feedback.
	-	1:0	Reserved.
<b>13h</b>	<b>YGAIN</b>	<b>7:0</b>	<b>Default : 0xC8</b> <b>Access : R/W</b>

**Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	YGAIN	7:0	Luma Gain for U/V Demodulation. Out=In*Gain+16. 0: 0. 128: 1. 255: 1.992.
14h	<b>CBGAIN</b>	<b>7:0</b>	<b>Default : 0x96</b> <b>Access : R/W</b>
	CBGAIN	7:0	Cb Gain for U/V Demodulation.
15h	<b>CRGAIN</b>	<b>7:0</b>	<b>Default : 0x6A</b> <b>Access : R/W</b>
	CRGAIN	7:0	Cr Gain for U/V Demodulation.
16h	<b>DITHCTRLA</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	CTSTDITHEN	6	Dithering when Contrast Adjustment.
	CTSTDITHPOS	5:4	Dithering Position (Offset) of Contrast.
	-	3	Reserved.
	SATDITHEN	2	Dithering when Saturation Adjustment.
	SATDITHPOS	1:0	Dithering Position (Offset) of Saturation.
17h	<b>DITHCTRLB</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7	Reserved.
	YDEMDITHEN	6	Dithering when Demodulation Y-Gain.
	YDEMDITHPOS	5:4	Dithering Position (Offset) of Y Gain.
	-	3	Reserved.
	CDEMDITHEN	2	Dithering when Demodulation C-Gain.
	CDEMDITHPOS	1:0	Dithering Position (Offset) of C Gain.
18h	<b>HORSTPOS</b>	<b>7:0</b>	<b>Default : 0xC0</b> <b>Access : R/W</b>
	HORSTPOS[7:0]	7:0	Horizontal Starting Position. 0..255 : -128..127.
19h	<b>FRHTOTL</b>	<b>7:0</b>	<b>Default : 0x8D</b> <b>Access : R/W</b>
	FRHTOTL	7:0	Free Run HSYNC Total Low Byte.
1Ah	<b>FRHTOTH</b>	<b>7:0</b>	<b>Default : 0x03</b> <b>Access : R/W</b>
	FRHTOTH	7:0	Free Run HSYNC Total High Byte.
1Bh	<b>PHSDETCFG</b>	<b>7:0</b>	<b>Default : 0x83</b> <b>Access : R/W</b>
	PHSDETEN	7	Line-Lock Phase Detection Enable.
	PHSDETINV	6	Output Inverse.

**Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	-	5:3	Reserved.
	PHSDETSFT	2:0	Shift Bit Number. 000: Only output integer. 001: Output shift right 1 bit. ... 111: Output shift right 7 bit.
	<b>CTRLSWCH</b>	<b>7:0</b>	<b>Default : 0xF0</b> <b>Access : R/W</b>
	HSFRAFEC	7	H-SYNC from AFEC.
	VSFRAFEC	6	V-SYNC from AFEC.
	BLKFRAFEC	5	Black Level from AFEC.
	DEGFRAFEC	4	Demodulation Degree from AFEC.
	-	3:2	Reserved.
	STDSEL	1:0	NTSC/PAL Decision. 01: force NTSC. 10: force PAL. Other: Auto detect.
<b>20h</b>	<b>COMB2DCFGA</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:0	Reserved.
<b>21h</b>	<b>COMB2DCFGB</b>	<b>7:0</b>	<b>Default : 0xD4</b> <b>Access : R/W</b>
	CRMATRP_EN	7	C-Trap of C Enable.
	NCHMD_Y[2:0]	6:4	Notch Mode of Y.
	CHRMFLT_EN	3	Chroma Median Filter Enable. 0: Off 1: Enable
	NCHMD_C[2:0]	2:0	Notch Mode of C.
<b>22h</b>	<b>COMB2DCFGC</b>	<b>7:0</b>	<b>Default : 0x83</b> <b>Access : R/W</b>
	LNENDPOS	7:4	Line End Offset. 0~15: -8~7.
	SHARP2DMD	3:2	Sharpness Mode of 2D Comb. 00: Off. 01: Mode 1. 10: Mode 2. 11: Mode 3.
	CDEMCHK	1	Chroma Vertical Check (dem).
	FORCE5LN	0	Force use 5 Line even in 1D.
<b>23h</b>	<b>HDYGAIN</b>	<b>7:0</b>	<b>Default : 0x40</b> <b>Access : R/W</b>

**Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	HDYGAIN	7:0	Gain of Chroma Trap for Hanging Dots.
24h	<b>HDCGAIN</b>	<b>7:0</b>	<b>Default : 0x20</b> <b>Access : R/W</b>
	HDCGAIN	7:0	Gain of Chroma Trap for Hanging Dots.
25h	<b>ETPREF</b>	<b>7:0</b>	<b>Default : 0x18</b> <b>Access : R/W</b>
	ETPREF	7:0	Gain of Chroma Trap for Hanging Dots.
26h	<b>ETPTHH</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	ETPTHH	7:0	Horizontal Entropy Threshold for Chroma Trap in 2D Comb.
27h	<b>ETPTHV</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	ETPTHV	7:0	Vertical Entropy Threshold for Chroma Trap in 2D Comb.
28h	<b>THDEM</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>
	THDEM	7:0	Thresholds for 2D Comb Filter; check separated chroma complement with up/down line or not.
29h ~ 2Eh	-	7:0	Reserved.
2Fh	<b>IFCOEF</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	IFCOEF	7:0	If compensation Coefficient. 2-bit integer, 6-bit fraction. $Crma=C\_cn-(Coef*(C\_left+C\_right))$ .
30h ~ 3Fh	-	7:0	Reserved.
40h	<b>HVDETCFG</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	SENSYNCLVL	7:5	Sensitivity of SYNC Level Detect.
	-	4:3	Reserved.
	BLNKDETM	2	Blank Level Detect Mode. 0: Either 240 or 252. 1: 230~262 is possible.
	VDETM	1:0	Vertical Timing Detect Mode. 00, 01: Auto detect. 10: force 525 line system. 11: force 625 line system.
41h	<b>SENSSIGDET</b>	<b>7:0</b>	<b>Default : 0x08</b> <b>Access : R/W</b>
	SENSSIGDET	7:0	Sensitivity of Signal Detect.
42h	<b>SYNCLVTLRN</b>	<b>7:0</b>	<b>Default : 0xFF</b> <b>Access : R/W</b>
	SYNCLVTLRN	7:0	SYNC Level Tolerance.



**Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
43h	<b>VCRCOASTLEN</b>	<b>7:0</b>	<b>Default : 0x60</b> <b>Access : R/W</b>
	VCRCOASTLEN	7:0	VCR Coast Length.
44h	<b>REGHBIDLY</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	REGHBIDLY	7:0	Horizontal Blanking Region Delay. 0 ... 255 : Delay -128 .. 127 pixels.
45h ~ 47h	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
48h	<b>DEGDETCFG</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	YCPIPE	7:6	Y/C Pipe Delay.
	DEGPIPE	5:4	Degree Pipe Delay.
	DEG1LNMD	3	Using just one line's Burst Determine the Degree.
	DEGSENS	2:0	Sensitivity of Degree Detect. 000: Directly use AFEC degree. 001: Tolerate 16384 errors. 010: Tolerate 8192 errors. 011: Tolerate 4096 errors. 100: Tolerate 2048 errors. 101: Tolerate 1024 errors. 110: Tolerate 512 errors. 111: Tolerate 256 errors.
49h	<b>THBURST</b>	<b>7:0</b>	<b>Default : 0x1E</b> <b>Access : R/W</b>
	THBURST	7:0	Degree Detection Tolerance Registers.
4Ah	<b>TLRNSWCHERR</b>	<b>7:0</b>	<b>Default : 0xC8</b> <b>Access : R/W</b>
	TLRNSWCHERR	7:0	Degree Detection Tolerance Registers.
4Bh	<b>HSLEADRGN</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	HSLEADRGN	7:0	HSYNC Leading Edge Range, for Even/Odd Detect.
4Ch ~ 4Fh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
50h	<b>TIMDETCFGA</b>	<b>7:0</b>	<b>Default : 0x07</b> <b>Access : R/W</b>
	-	7:4	Reserved.
	AUTOSTOPSYNC	3	Automatic Stop H/V Sync when No Input.

**Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	LNFREEMD	2:0	Line Buffer Free Run Mode. 000: Off (always synchronize). 001: 909 return. 010: 910 return. 011: 917 return. 100: 1127 return. 101: 1135 return. 110: Decided by register. 111: Automatic.
51h	<b>TIMDETCFGB</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	STBCNTMD	7:6	Stable Counter Mode. 00: div 16. 01: div 32. 10: div 64. 11: div 128.
	HSSTBDEC	5:0	HSYNC Stable Counter Decrease Speed.
52h	<b>HRETPOSL</b>	<b>7:0</b>	<b>Default : 0x8E</b> <b>Access : R/W</b>
	HRETPOSL	7:0	Horizontal Return Position in Line Buffer Free Run Mode.
53h	<b>HRETPOSH</b>	<b>7:0</b>	<b>Default : 0x03</b> <b>Access : R/W</b>
	HRETPOSH	7:0	Horizontal Return Position in Line Buffer Free Run Mode.
54h	<b>TILTTLRN</b>	<b>7:0</b>	<b>Default : 0x02</b> <b>Access : R/W</b>
	TILTTLRN	7:0	Line Position Tilt Tolerance.
55h	<b>JITTLRN3D</b>	<b>7:0</b>	<b>Default : 0x08</b> <b>Access : R/W</b>
	JITTLRN3D	7:0	3D Timing Detection Tolerance.
56h	<b>LCKSTEP</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	LCKSTEP	7:0	3D Lock Counter Go Back Distance when SYNC Unstable.
57h	<b>LCK3DTHU</b>	<b>7:0</b>	<b>Default : 0x33</b> <b>Access : R/W</b>
	LCK3DTHU	7:0	3D Timing Detection Threshold.
58h	<b>LCK3DTHL</b>	<b>7:0</b>	<b>Default : 0x11</b> <b>Access : R/W</b>
	LCK3DTHL	7:0	3D Timing Detection Threshold.
59h	<b>JITTLRN1</b>	<b>7:0</b>	<b>Default : 0x08</b> <b>Access : R/W</b>
	JITTLRN1	7:0	Tolerance of H-SYNC Jitter.
5Ah	<b>JITTLRN2</b>	<b>7:0</b>	<b>Default : 0x20</b> <b>Access : R/W</b>
	JITTLRN2	7:0	Tolerance of H-SYNC Jitter.
5Bh	<b>HSLCKTHU</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>

**Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	HSLCKTHU	7:0	Upper Bound Threshold of Hysteresis H-SYNC Lock Counter.
5Ch	<b>HSLCKTHL</b>	<b>7:0</b>	<b>Default : 0x08</b> <b>Access : R/W</b>
	HSLCKTHL	7:0	Lower Bound Threshold of Hysteresis H-SYNC Lock Counter.
5Dh	<b>HSCHGTLRN</b>	<b>7:0</b>	<b>Default : 0xFF</b> <b>Access : R/W</b>
	HSCHGTLRN	7:0	Tolerance of HSYNC Counter Change Times. Even HSYNC locked, but if timing drifted too many times, systme still should turn off 2D/3D. 00h: immediately stop 2D/3D when HsChg happen. FFh: Never stop 2D/3D if HsLock.
5Eh	<b>SYNCDLY</b>	<b>7:0</b>	<b>Default : 0x14</b> <b>Access : R/W</b>
	SYNCDLY	7:0	H SYNC (from Decoder to Scaler) Pipe Delay.
5Fh	-	7:0	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
60h	<b>IMGCTRL</b>	<b>7:0</b>	<b>Default : 0xF0</b> <b>Access : R/W</b>
	COLKILLMD	7:6	Color Kill Mode. 00: Off. 01: Auto. 10, 11: Decided by MCU.
	CGMODE	5:4	Auto Chroma Gain Mode. 00: Off. 01: Auto. 10, 11: Manual.
	AC_MD	3	Auto Contrast Mode. 0: Double at most. 1: 4 times at most.
	AUTO_CSTS	2	Auto Contrast Adjustment.
	-	1	Reserved.
	AUTO_SAT	0	Auto Saturation Adjustment.
61h	<b>RSPNTIME</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>
	RSPNTIME	7:0	Response Time of Contrast/Brightness Adjust. 0... 255 => 1... 256 field.
62h	<b>REGBSTHGHT</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	REGBSTHGHT	7:0	Burst Height for Auto Chroma Gain. 0: Auto, 112 for NTSC and 117 for PAL. Other: use RegBstHght/DetBstHght as C Gain.
63h	<b>REGCTST</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>

<b>Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)</b>			
Index	Name	Bits	Description
	REGCTST	7:0	Contrast adjustment Coefficient. 0... 255 => 0... (255/128).
64h	<b>REGBRHT</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	REGBRHT	7:0	Brightness adjustment Coefficient. 0... 255 => -128... 127 in 8-bit precision.
65h	<b>REGSAT</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	REGSAT	7:0	Saturation adjustment Coefficient. 0... 255 => (0... 255)/128.
66h	<b>CKTHU</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	CKTHU	7:0	Upper Bound Threshold of Color Kill.
67h	<b>CKTHL</b>	<b>7:0</b>	<b>Default : 0x30</b> <b>Access : R/W</b>
	CKTHL	7:0	Lower Bound Threshold of Color Kill.
68h	<b>CRMAGAINL</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	CRMAGAINL	7:0	Chroma Gain Value for Manu Chroma Gain.
69h	<b>CRMAGAINH</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	CRMAGAINH	7:0	Chroma Gain Value for Manu Chroma Gain.
6Ah	<b>MAXLUMA</b>	<b>7:0</b>	<b>Default : 0xB0</b> <b>Access : R/W</b>
	MACLUMA	7:0	Max Luminance for Auto Contrast Adjust.
6Bh	<b>MAXSAT</b>	<b>7:0</b>	<b>Default : 0xC0</b> <b>Access : R/W</b>
	MAXSAT	7:0	MAX Saturation for Auto Saturation Adjust.
6Ch	<b>MAXCRMA</b>	<b>7:0</b>	<b>Default : 0xC0</b> <b>Access : R/W</b>
	MAXCRMA	7:0	MAX Chrominance for Auto Saturation Adjust.
6Dh	<b>SNOWDELAY</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	SNOWDELAY	7:0	Latency of Snow Output after Signal Missing.
6Eh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
6Fh	<b>CBCRLPCFG</b>	<b>7:0</b>	<b>Default : 0x04</b> <b>Access : R/W</b>
	CTIIRMD	7:6	IIR Coefficient for CTI. 00: 1/4. 01: 1/8. 10: 1/16. 11: 1/32.

**Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	CTIMODE	5:4	CTI Mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.
	YPIPDLY	3:2	Luma Pipe Delay. 00: -1 cycle. 01: 0 cycle. 10: 1 cycle. 11: 2 cycle.
	CBCRLPMD	1:0	Cb/Cr Low Pass Mode. 0: Off. 01: Cut off at 2.0MHz. 10: Cut off at 1.5MHz. 11: Cut off at 1.0MHz
<b>70h</b>	<b>COMBSTATUSA</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : Write one clear</b>
	HSLOCK	7	HSYNC Lock Happen.
	LOCK3D	6	Good Timing (Lock3D) Happen.
	-	5:4	Reserved.
	HSLOCKZ	3	HSYNC Unlock Happen.
	LOC3DZ	2	Good Timing (Lock3D) Disappear.
	HSCHG	1	H-SYNC Counter Change.
	-	0	Reserved.
<b>71h</b>	<b>COMBSTATUSB</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : Write one clear</b>
	-	7:6	Reserved.
	CCHNLACT	5	C-channel Active (maybe S-Video Input).
	CCHNLACT	4	C-channel Quiet (maybe CVBS Input0).
	-	3	Reserved.
	FLDCNTCHG	2	Field Counter Change.
	PALSWCHERR	1	PAL Switch Error.
	DEGERR	0	Degree Error (Degree Detect).
<b>72h</b>	<b>COMBSTATUSC</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	LN525	7	525 Line System.
	LN625	6	625 Line System.
	F358	5	3.58 MHz System.
	F443	4	4.43 MHz System.

**Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)**

Index	Name	Bits	Description
	NOINPUT	3	No Input.
	VDOMD	2:0	Video Mode. 000: NTSC(M). 001: NTSC(443). 010: PAL (M). 011: PAL(B,D,G,H,I,N). 100: PAL(Nc). 101: PAL(60). 110: Input without Burst. 111: Unknown.
73h	<b>DETBLANKLVL</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	DETBLANKLVL	7:0	Detected Blanking Level.
74h	<b>CURBLANKLVL</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	CURBLANKLVL	7:0	Detected Blanking Level.
75h	<b>DETSYNCLVL</b>	<b>7:0</b>	<b>Default :-</b> <b>Access : RO</b>
	DETSYNCLVL	7:0	Detected Sync Level.
76h	<b>DETSYNCHGHT</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	DETSYNCHGHT	7:0	Detected SYNC Height.
77h	<b>DETBURSTHGT</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	DETBURSTHGT	7:0	Detected Burst Level.
78h	<b>DETHORTOTALL</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	DETHORTOTALL	7:0	
79h	<b>DETHORTOTALH</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : R</b>
	DETHORTOTALH	7:0	
7Ah ~ 7Ch	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
7Dh	<b>COMBCTRL</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	COMBCTRL	7:0	Some Control Signals for FPGA.
7Eh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.
7Fh	<b>FPGACTRL</b>	<b>7:0</b>	<b>Default : 0xE0</b> <b>Access : R/W</b>
	FPGACTRL	7:0	Some Control Signals for FPGA.
80h ~ 9Fh	-	<b>7:0</b>	<b>Default : -</b> <b>Access : -</b>
	-	7:0	Reserved.

## DIGITAL PWM Register (Bank = 04)

DIGITAL PWM Register (Bank = 04)				
Index	Name	Bits	Description	
01h ~ 6Ah	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
6Bh	PROTECT_BIT	7:0	Default : 0x00	Access : R/W
	PROTECT_BIT	7:0	Have to set as 1 in that could view all PWM register setting.	
6Ch	STUS_RPRT	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	STUS_RPRT[2]	2	1: FAULTZ is high.	
	STUS_RPRT[1]	1	1: FB2 mode is on.	
	STUS_RPRT[0]	0	1: VIN is OK.	
6Dh	PWM_SWCH	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM_SWCH[1:0]	1:0	Control PWM on/off; must set to "00" or "11". 00: PWM off. 11: PWM on. Others: Off (not recommended).	
6Eh	OP_MD	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	PWM_SWRST	6	Software-Reset bit to reset PWM. 0: No action. 1: Software reset and remain in initial state using a single pulse.	
	VSYNC_PLRTY_SEL	5	VSYNC polarity setting. 0: Same polarity to VSYNC. 1: Opposite polarity.	
	VSYNC_SEL	4	Use TCON's VSYNC for VSYNC-mode. 0: Use normal VSYNC. 1: Use TCON's VSYNC.	
	PWM_EN	3	PWM function on/off. 0: Use external controller. 1: User internal controller.	
	FAULTZ_H_MD_EN	2	FAULTZ High Mode on/off. 0: Off. 1: On.	
	VSYNC_MD_EN	1	VSYNC Mode on/off. 0: Off. 1: On.	

### DIGITAL PWM Register (Bank = 04)

Index	Name	Bits	Description
	BRST_MD_EN	0	Burst Mode on/off. 0: Off. 1: On.
6Fh	VIN_STAB_CNT	7:0	Default : 0x0A
	VIN_STAB_CNT	7:0	VIN Stable Count number.
70h	VIN_OV_CNT	7:0	Default : 0x0A
	VIN_OV_CNT	7:0	VIN Over-Voltage Count number.
71h	VIN_UV_CNT	7:0	Default : 0x0A
	VIN_UV_CNT	7:0	VIN Under-Voltage Count number.
72h	VIN_WRK_H_THRD	7:0	Default : 0xC3
	VIN_WRK_H_THRD	7:0	VIN Working High Threshold.
73h	VIN_STRTUP_H_THRD	7:0	Default : 0xBB
	VIN_STRTUP_H_THRD	7:0	VIN Startup High Threshold.
74h	VIN_STRTUP_L_THRD	7:0	Default : 0x99
	VIN_STRTUP_L_THRD	7:0	VIN Startup Low Threshold.
75h	VIN_WRK_L_THRD	7:0	Default : 0x90
	VIN_WRK_L_THRD	7:0	VIN Working Low Threshold.
76h	VIN_WAIT_CNT_L	7:0	Default : 0xFA
	VIN_WAIT_CNT[7:0]	7:0	VIN Waiting Count number (lower 8 bits).
77h	VIN_WAIT_CNT_H	7:0	Default : 0x00
	-	7:4	Reserved.
	VINWAIT_CNT[11:8]	3:0	VIN Waiting Count number (upper 4 bits)

**When 6E[2] = 0, please refer to the following as register settings of 78h ~ 7Bh:**

78h	FAULTZ_H_VAL	7:0	Default : 0xAA
	FAULTZ_H_VAL[7:0]	7:0	FAULTZ High boundary.
79h	FAULTZ_L_VAL	7:0	Default : 0x55
	FAULTZ_L_VAL[7:0]	7:0	FAULTZ Low boundary.
7Ah	FAULTZ_STB	7:0	Default : 0x0A
	FAULTZ_STB[7:0]	7:0	Counts for FAULTZ Stable.
7Bh	FAULTZ_DROP	7:0	Default : 0x0A
	FAULTZ_H_GO_LOW	7:0	Counts for FAULTZ High Go Low.

**When 6E[2] = 1, please refer to the following as register settings of 78h ~ 7Bh:**



### DIGITAL PWM Register (Bank = 04)

Index	Name	Bits	Description
78h	<b>FAULTZ_H_VALUE</b>	<b>7:0</b>	<b>Default : 0xAA</b> <b>Access : R/W</b>
	FB2_DET_TIME[7:0]	7:0	FB2 Detection Time after burst high when system is in FAULTZ high mode (lower 8 bits).
79h	<b>FAULTZ_L_VALUE</b>	<b>7:0</b>	<b>Default : 0x55</b> <b>Access : R/W</b>
	-	7:2	Reserved.
	FB2_DETECT_TIME[9:8]	1:0	FB2 Detection Time after burst high when system is in FAULTZ high mode (higher 2 bits).
7Ah	<b>FAULTZ_STB_CNT</b>	<b>7:0</b>	<b>Default : 0x0A</b> <b>Access : R/W</b>
	FB2_DET_FAIL_T	7:0	Counts for FB2 failure is True.
7Bh	<b>FAULTZ_DROP</b>	<b>7:0</b>	<b>Default : 0x0A</b> <b>Access : R/W</b>
	FB2_L_FAULTZ_H_MD	7:0	FB2 Low Bound in FAULTZ High Mode.
7Ch	<b>MSUR_OFST_L</b>	<b>7:0</b>	<b>Default : 0x0E</b> <b>Access : R/W</b>
	MSUR_OFST[7:0]	7:0	Measure Offset time to get Data (lower 8 bits).
7Dh	<b>MSUR_OFST_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:2	Reserved.
	MSUR_OFST[9:8]	1:0	Measure Offset time to get Data (higher 2 bits).
7Eh	<b>2US</b>	<b>7:0</b>	<b>Default : 0x48</b> <b>Access : R/W</b>
	2US_CNT	7:0	Counts for 2us.
7Fh	<b>2US_MSUR</b>	<b>7:0</b>	<b>Default : 0x14</b> <b>Access : R/W</b>
	2US_MSUR	7:0	Counts to get Data when PWM on time $\leq$ 2us.
80h	<b>FB1_COM</b>	<b>7:0</b>	<b>Default : 0xAA</b> <b>Access : RO</b>
	FB1_COM[7:0]	7:0	FB1 Command.
81h	<b>FB2_STRTUP</b>	<b>7:0</b>	<b>Default : 0xAA</b> <b>Access : R/W</b>
	FB2_STRTUP	7:0	Start-up FB2 Command.
82h	<b>FB2_SET</b>	<b>7:0</b>	<b>Default : 0xAA</b> <b>Access : R/W</b>
	FB2_SET	7:0	FB2 Command; adjust for continuous output adjusting.
83h	<b>CONT_AB</b>	<b>7:0</b>	<b>Default : 0xB7</b> <b>Access : R/W</b>
	CONT_A	7:4	A-value for Continuous-mode.
	CONT_B	3:0	B-value for Continuous-mode.
84h	<b>BRST_AB</b>	<b>7:0</b>	<b>Default : 0xB7</b> <b>Access : R/W</b>
	BRST_A	7:4	A-value for Burst-mode.
	BRST_B	3:0	A-value for Burst-mode.

### DIGITAL PWM Register (Bank = 04)

Index	Name	Bits	Description
85h	<b>STRK1_L</b>	<b>7:0</b>	<b>Default : 0xA9</b> <b>Access : R/W</b>
	STRK1_CNT[7:0]	7:0	1 <sup>st</sup> ignition and normal operation Count for PWM frequency; double buffer must fill-in from high to low.
86h	<b>STRK1_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:2	Reserved.
	STRK1 [9:8]	1:0	1 <sup>st</sup> Ignition and normal operation count for PWM frequency; double buffer must fill-in from high to low.
87h	<b>STRK1_LMT_L</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	STRK1_LMT[7:0]	7:0	Maximum duty for 1 <sup>st</sup> ignition and normal operation; count for PWM frequency (lower 8 bits).
88h	<b>STRK1_LMT_H</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-	7:2	Reserved.
	STRK1_LMT[9:8]	1:0	Maximum duty for 1 <sup>st</sup> ignition and normal operation; count for PWM frequency (higher 2 bits).
89h	<b>STRK2_L</b>	<b>7:0</b>	<b>Default : 0xA9</b> <b>Access : R/W</b>
	STRK2_CNT[7:0]	7:0	2 <sup>nd</sup> ignition count for PWM frequency; double-buffer must fill-in from high to low (lower 8 bits).
8Ah	<b>STRK2_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:2	Reserved.
	STRK2 [9:8]	1:0	2 <sup>nd</sup> ignition count for PWM frequency; double-buffer must fill-in from high to low (higher 2 bits).
8Bh	<b>STRK2_LMT</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	STRK2_LMT[7:0]	7:0	Maximum duty of 2 <sup>nd</sup> ignition; count for PWM frequency.
8Ch	<b>STRK2_LMT</b>	<b>7:0</b>	<b>Default : -</b> <b>Access : RO</b>
	-	7:2	Reserved.
	STRK2_LMT[9:8]	1:0	Maximum duty for 2 <sup>nd</sup> ignition; count for PWM frequency.
8Dh	<b>CNT_MD</b>	<b>7:0</b>	<b>Default : 0x55</b> <b>Access : R/W</b>
	FB2_MD_CTRL	7:4	Counts for entering FB2 Mode Control.
	FAULTZ_OVP	3:0	Counts for FAULTZ Over-Voltage Protection.
8Eh	<b>BRST_L</b>	<b>7:0</b>	<b>Default : 0x80</b> <b>Access : R/W</b>
	BRST_CNT[7:0]	7:0	Counts for Burst-mode frequency (lower 8 bits; filling sequence: 8Fh, 8Eh, 91h, 90h).
8Fh	<b>BRST_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>

### DIGITAL PWM Register (Bank = 04)

Index	Name	Bits	Description
	-	7:2	Reserved.
	BRST_CNT[9:8]	1:0	Counts for Burst-mode frequency (higher 2 bits; filling sequence: 8Fh, 8Eh, 91h, 90h).
90h	<b>BRST_DUTY_L</b>	<b>7:0</b>	<b>Default : 0x10</b> <b>Access : R/W</b>
	BRST_DUTY[7:0]	7:0	Counts for Burst-mode Duty (lower 8 bits; filling sequence: 8Fh, 8Eh, 91h, 90h).
91h	<b>BRST_DUTY_H</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	-	7:2	Reserved.
	BRST_DUTY[9:8]	1:0	Counts for Burst-mode Duty (higher 2 bits; filling sequence: 8Fh, 8Eh, 91h, 90h).
92h	<b>STRK1_TIME_L</b>	<b>7:0</b>	<b>Default : 0x50</b> <b>Access : R/W</b>
	STRK1_TIME[7:0]	7:0	Counts for 1 <sup>st</sup> ignition Time (lower 8 bits).
93h	<b>STRK1_TIME_M</b>	<b>7:0</b>	<b>Default : 0xC3</b> <b>Access : R/W</b>
	STRK1_TIME[15:8]	7:0	Counts for 1 <sup>st</sup> Ignition Time (middle 8 bits).
94h	<b>STRK1_TIME_H</b>	<b>7:0</b>	<b>Default : 0x00</b> <b>Access : R/W</b>
	-	7:4	Reserved.
	STRK1_TIME[19:16]	3:0	Counts for 1 <sup>st</sup> ignition time (higher 4 bits).
95h	<b>TTAL_STRK_TIME_L</b>	<b>7:0</b>	<b>Default : 0x38</b> <b>Access : R/W</b>
	TTAL_STRK_TIME[7:0]	7:0	Counts for 1 <sup>st</sup> ignition time + 2 <sup>nd</sup> ignition time (lower 8 bits).
96h	<b>TTAL_STRK_TIME_M</b>	<b>7:0</b>	<b>Default : 0xC1</b> <b>Access : R/W</b>
	TTAL_STRK_TIME[15:8]	7:0	Counts for 1 <sup>st</sup> ignition time + 2 <sup>nd</sup> ignition time (middle 8 bits).
97h	<b>TTAL_STRK_TIME_H</b>	<b>7:0</b>	<b>Default : 0x01</b> <b>Access : R/W</b>
	-	7:4	Reserved.
	TTAL_STRK_TIME[19:16]	3:0	Counts for 1 <sup>st</sup> ignition time + 2 <sup>nd</sup> ignition time (higher 4 bits).
98h	<b>BRST_RAMP1</b>	<b>7:0</b>	<b>Default : 0x22</b> <b>Access : Reserved</b>
	BRST_RAMP1[7:0]	7:0	Burst-mode Ramp control (lower 8 bits).
99h	<b>BRST_RAMP2</b>	<b>7:0</b>	<b>Default : 0x11</b> <b>Access : Reserved</b>
	PWM_MAX_DUTY	7	PWM Maximum Duty. 0: STRIKE minus 16. 1: STRIKE minus 32.
	STEPS	6:4	Counts for Steps.
	BRST_RAMP1[11:8]	3:0	Burst-mode Ramp control (higher 4 bits). Four steps: 99[3:1], {99[0], 98[7:6]}, 98[5:3], 98[2:0].

### DIGITAL PWM Register (Bank = 04)

Index	Name	Bits	Description	Access
9Ah	<b>KEY_PRTEC</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	KEY_PRTEC	7:0	Key, code=CF.	
9Bh	<b>FAIL_STUS</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	FAIL_SAFE_ON	7	Fail-Safe finds PWM is over max-on time.	
	FAULTZ_H_MD_FB2_F	6	FAULTZ High-Mode, FB2 Fail.	
	FB1_OVP	5	FB1 Over-Voltage Protection while FAULTZ is high.	
	STRK_FAIL	4	Unable to force FAULTZ=1 after 2-step Striking.	
	FAULTZ_ABNRM	3	FAULTZ accidentally goes from high to low.	
	VIN_OV	2	VIN Over-Voltage.	
	VIN_UV	1	VIN Under-Voltage.	
	STRTUP_VIN_F	0	Startup VIN Fail.	
9Ch	<b>SAR_FB2_DAT</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	SAR_FB2_DAT	7:0	SAR FB2 Data.	
9Dh	<b>SAR_FB1_DAT</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	SAR_FB1_DAT	7:0	SAR FB1 Data.	
9Eh	<b>SAR_FAULTZ_DAT</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	SAR_FAULTZ_DAT	7:0	SAR FAULTZ Data.	
9Fh	<b>SAR_VIN_DAT</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	SAR_VIN_DAT	7:0	SAR VIN Data.	
A0h	<b>DUTY_RPRT1</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	DUTY_RPRT1[7:0]	7:0	PWM Duty.	
A1h	<b>DUTY_RPRT2</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	DUTY_RPRT2[7:0]	7:0	PWM Duty.	
A2h	<b>DUTY_RPRT3</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	-	7:4	Reserved.	
	DUTY_RPRT3[5:0]	5:0	PWM Duty.	
A4h	<b>SAR_SET1</b>	<b>7:0</b>	<b>Default : 0x09</b>	<b>Access : R/W</b>
	FS_Q2_EN	7	Enable Q2-Fail Safe.	
	FS_Q1_EN	6	Enable Q1-Fail Safe.	
	SAR_CLK_SEL	5	Select SAR Clock source. 0: PWM clock. 1: MPLL_CLK_OUT.	
	SAR_CLK_DIV_RATIO	4:0	Divide Ratio for SAR Clock.	

### DIGITAL PWM Register (Bank = 04)

Index	Name	Bits	Description	Access
A5h	<b>SAR_SET2</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	-	7:4	Reserved.	
	SAR_CH_SEL	3:2	Channel Select for SAR.	
	SAR_DEBUNCE_SET	1:0	De-bounce Setting for SAR.	
A6h	<b>SAR_SET3</b>	<b>7:0</b>	<b>Default : 0x0B</b>	<b>Access : R/W</b>
	SAR_SAMPLE_PRD	7:0	System clock counts for Sample Period.	
A7h	<b>SAR_SET4</b>	<b>7:0</b>	<b>Default : 0x30</b>	<b>Access : R/W</b>
	C1_Q2	7	Setting for programmable IO.	
	C1_Q1	6	Setting for programmable IO.	
	C0_Q2	5	Setting for programmable IO.	
	C0_Q1	4	Setting for programmable IO.	
	EPD_Q2	3	Enable input PAD_Q2 pull-down (default unused).	
	EPD_Q1	2	Enable input PAD_Q1 pull-down (default unused).	
	EN33V_DPWM	1	Enable 3.3V supply for AVDD_SAR.	
SAR_TST	0	Set SAR ADC input to zero.		
ABh	<b>HSYNC_PLL_SET</b>	<b>7:0</b>	<b>Default : 0x93</b>	<b>Access : R/W</b>
	USE_CLKDIV_EN	7	Enable Bit for using Clock Divider instead of using PLL. 0: Disable. 1: Enable.	
	PLL_LOCK	6	PLL Lock.	
	STRK1_SEL	5	Choose to use STRIKE1 or synchronized STRIKE1.	
	CLKIN_SEL	4	Select to use MPLL_CLK_OUT/(MPLL_CLK_OUT/2).	
	PLL_MODE	3:2	PLL-Mode setting.	
	HSYNC_SOURCE_SEL	1	Select-bit for Selecting the Source of HSYNC.	
	HSYNC_PLL_EN	0	Enable bit for HSYNC PLL.	
ACh	<b>PLL_CD</b>	<b>7:0</b>	<b>Default : 0x00</b>	<b>Access : R/W</b>
	PLL_M_CD	7:4	PLL M-Code; must be >0.	
	PLL_N_CD	3:0	PLL N-Code; must be >0.	
ADh	<b>PLL_STUS1</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	PLL_STUS_RPRT	7:0	HSYNC PLL Status Report.	
AEh	<b>PLL_STUS2</b>	<b>7:0</b>	<b>Default : -</b>	<b>Access : RO</b>
	HSYNC_IN	7	Monitor Input HSYNC.	
	PLL_STUS_RPRT	6:0	HSYNC PLL Status Report.	
AFh	<b>DIVD_RATIO</b>	<b>7:0</b>	<b>Default : 0x30</b>	<b>Access : R/W</b>

### DIGITAL PWM Register (Bank = 04)

Index	Name	Bits	Description
	HSYNC_DIVD_RATIO	7:0	Divide-Ratio while PLL is in divider-mode.
<b>B0h</b>	<b>WDT_L</b>	<b>7:0</b>	<b>Default : 0x00</b>   <b>Access : R/W</b>
	WDT[7:0]	7:0	Counts for WDT; (wanted PWM maximum on-time)/(BIU Clock) (lower 8 bits).
<b>B1h</b>	<b>WDT_H</b>	<b>7:0</b>	<b>Default : 0x00</b>   <b>Access : R/W</b>
	-	7:6	Reserved.
	WDT[9:8]	1:0	Counts for WDT; (wanted PWM maximum on-time) / (BIU Clock) (higher 2 bits).
<b>B2h</b>	<b>PLL_SET</b>	<b>7:0</b>	<b>Default : 0x20</b>   <b>Access : R/W</b>
	-	7:6	Reserved.
	HSYNC_SAFE_MD	5	HSYNC Safe-Mode.
	PLL_CLAMP_RATIO	4:0	PLL Clamp Value.
<b>B3h ~ FFh</b>	-	<b>7:0</b>	<b>Default : -</b>   <b>Access : -</b>
	-	7:0	Reserved.

### REGISTER TABLE REVISION HISTORY

Date	Bank	Register
11/15/05		Created first version.
03/16/06	00	0x1A
	02	0x19
	03	Removed

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